

FIG. 1

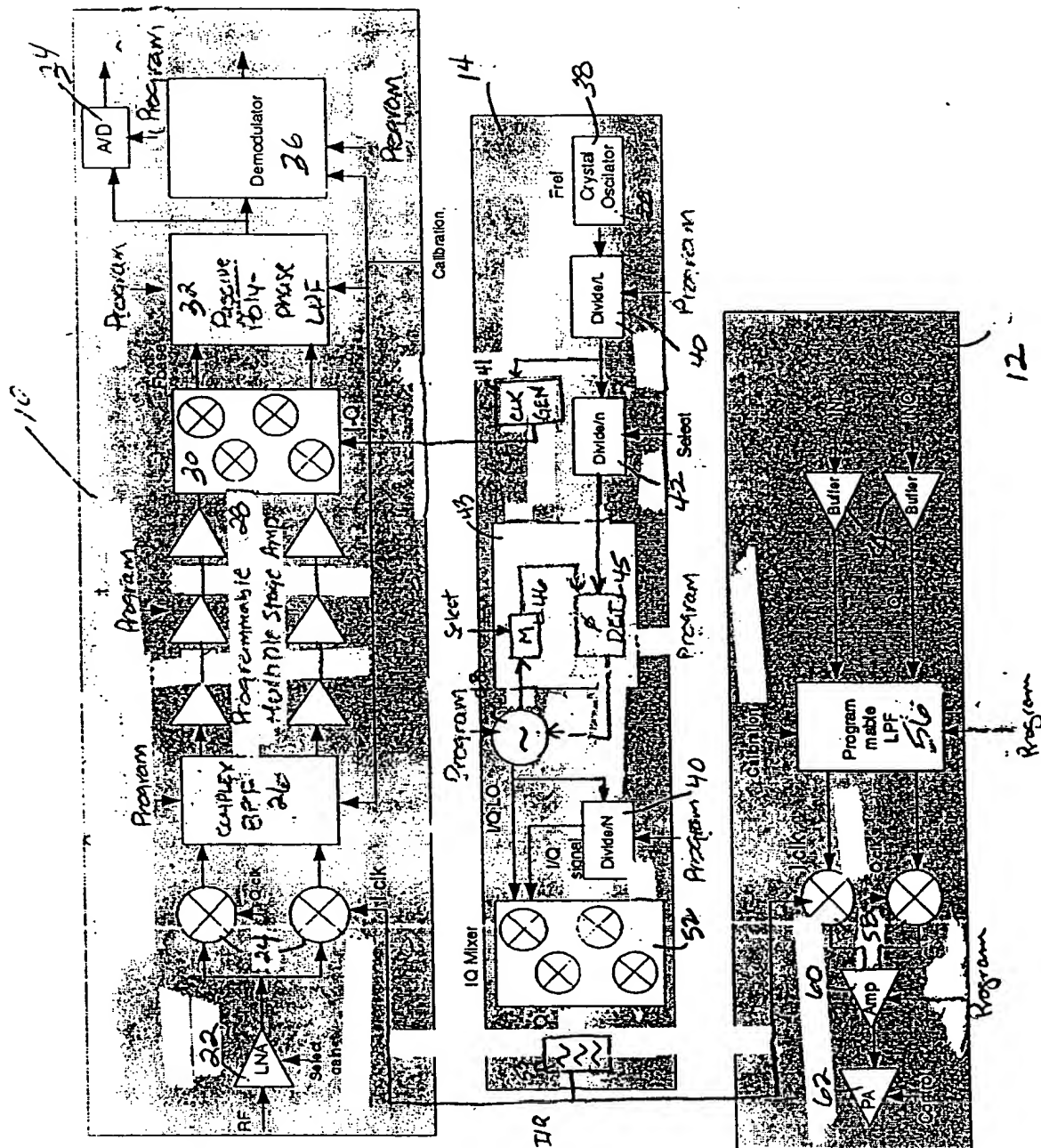


Fig. 2

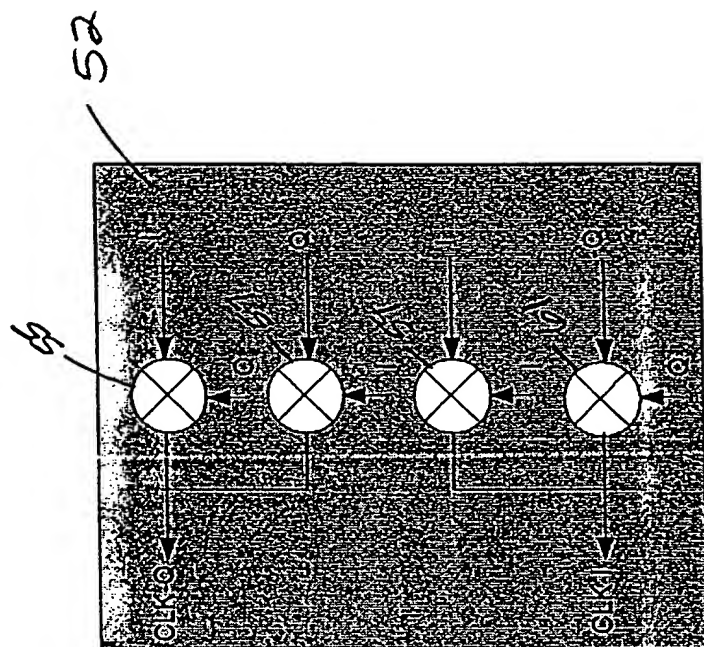


FIG. 3

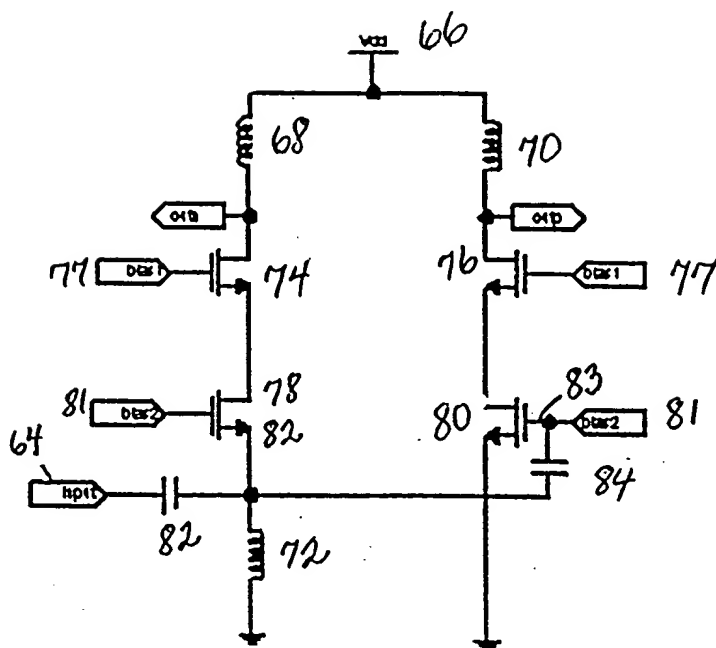


FIG. 4

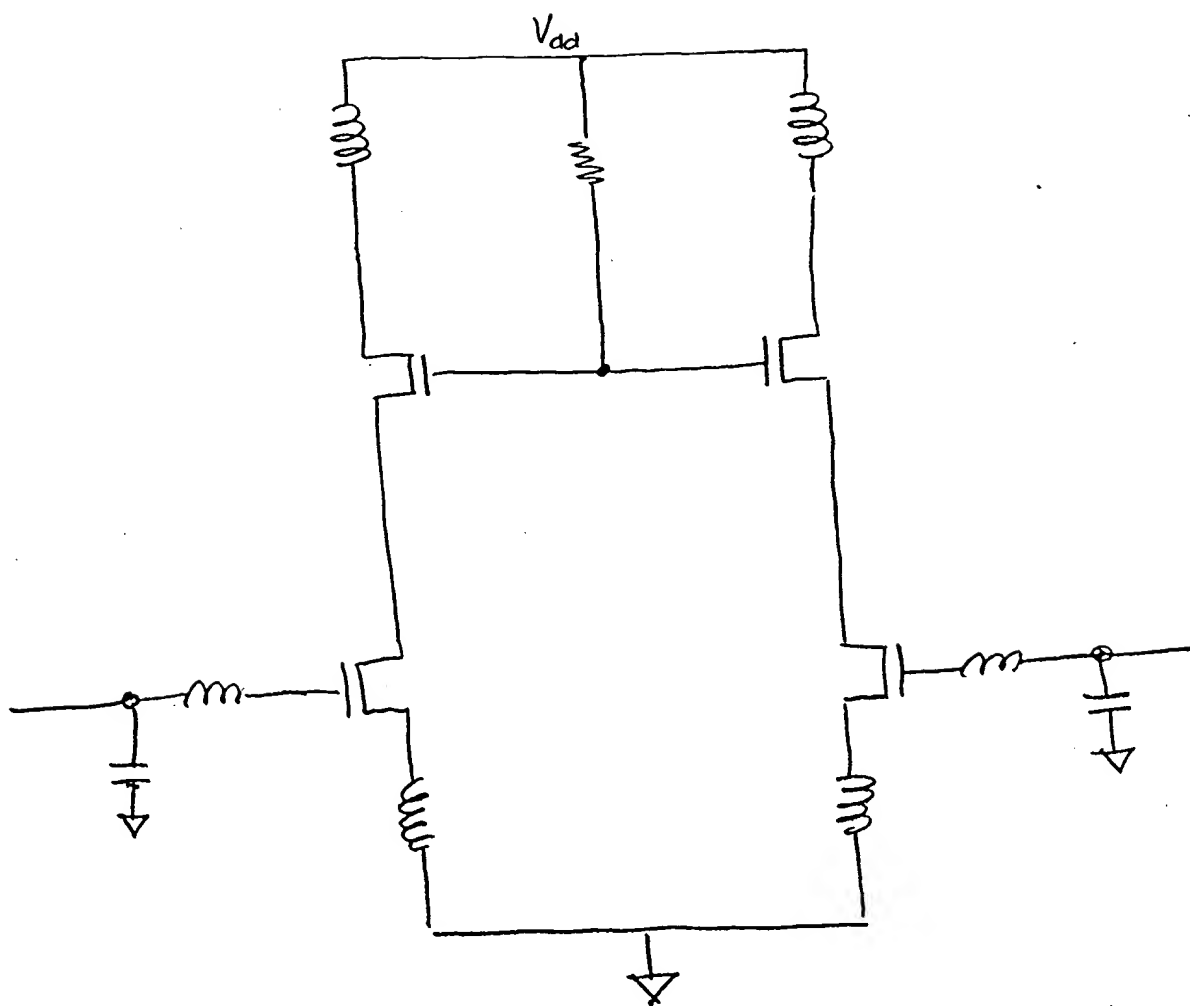


FIG. 4(a)

FIG. 5

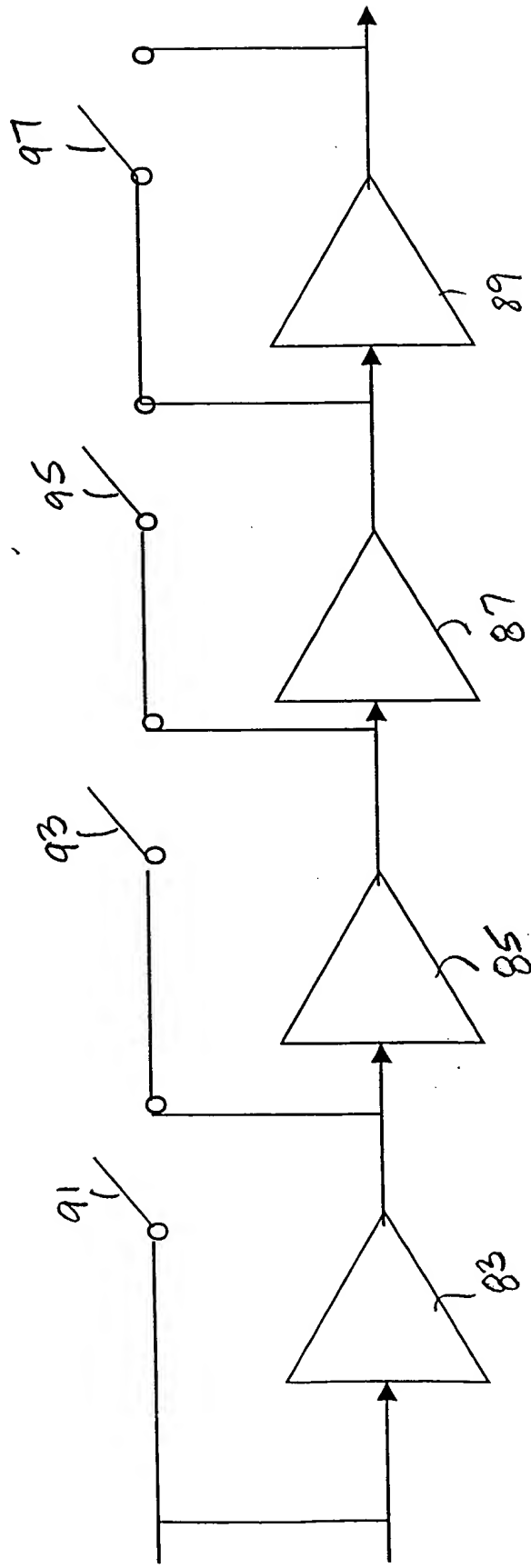


FIG. 5

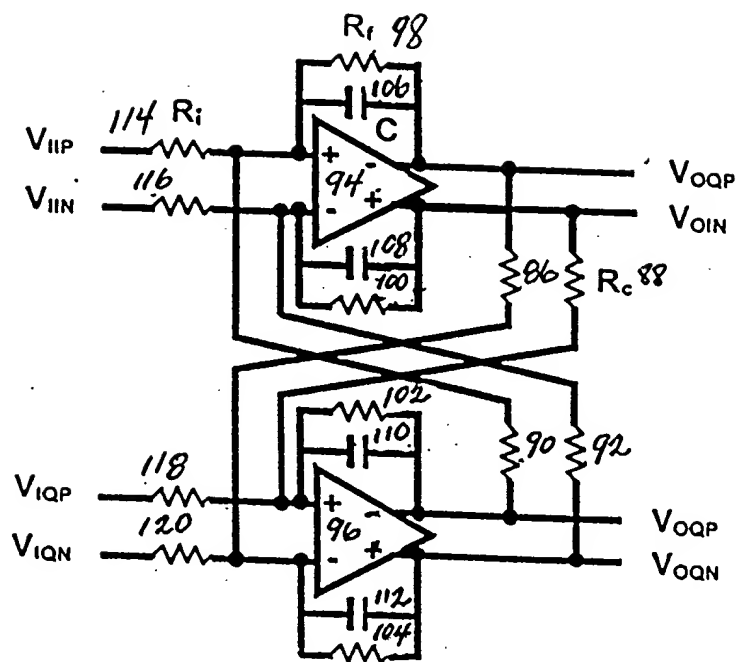


FIG. 6

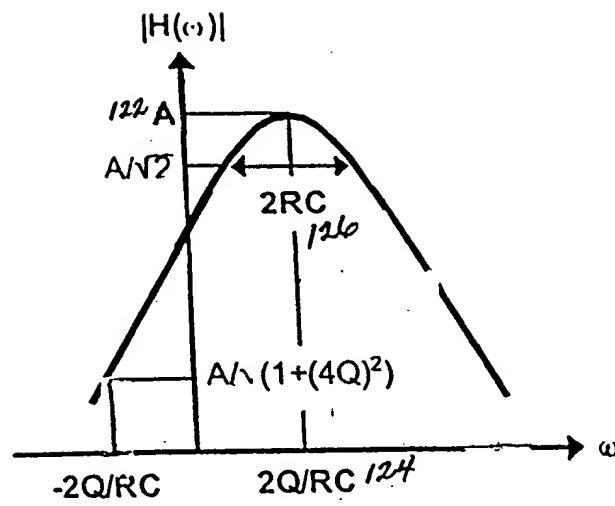


FIG. 7



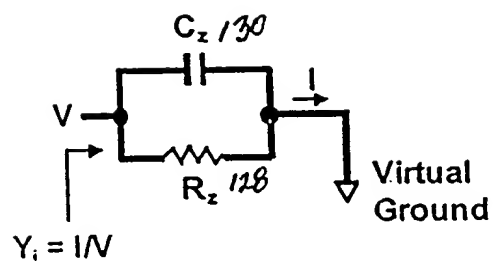


FIG. 8

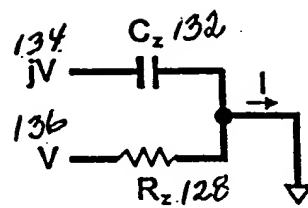


FIG. 9

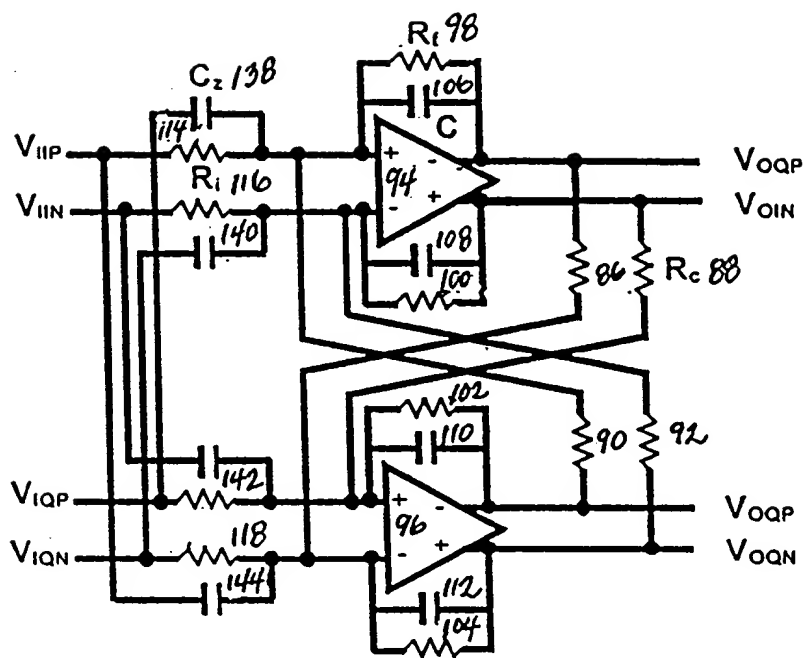


FIG. 10

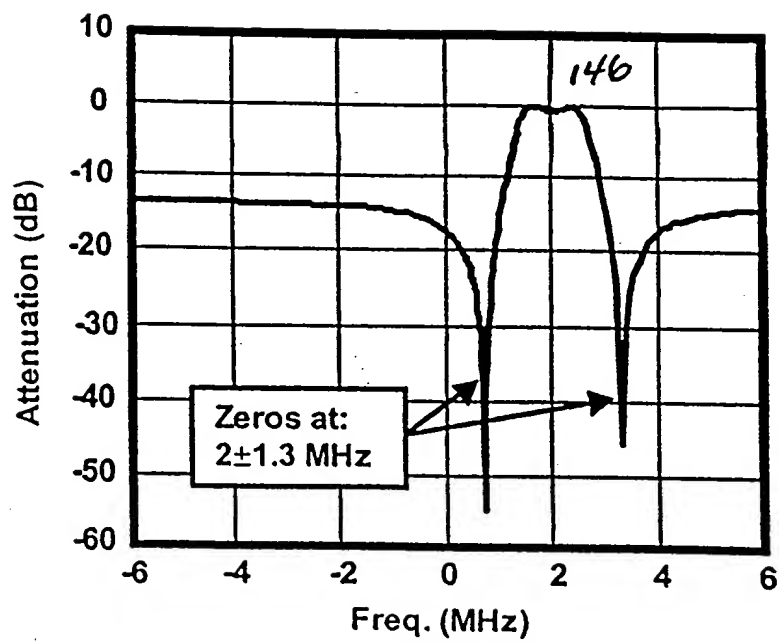


FIG. 11

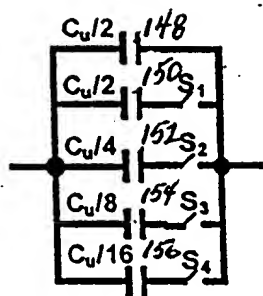


FIG. 12(a)

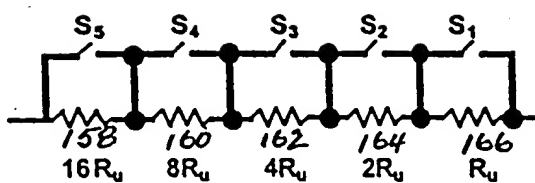


FIG. 12(b)

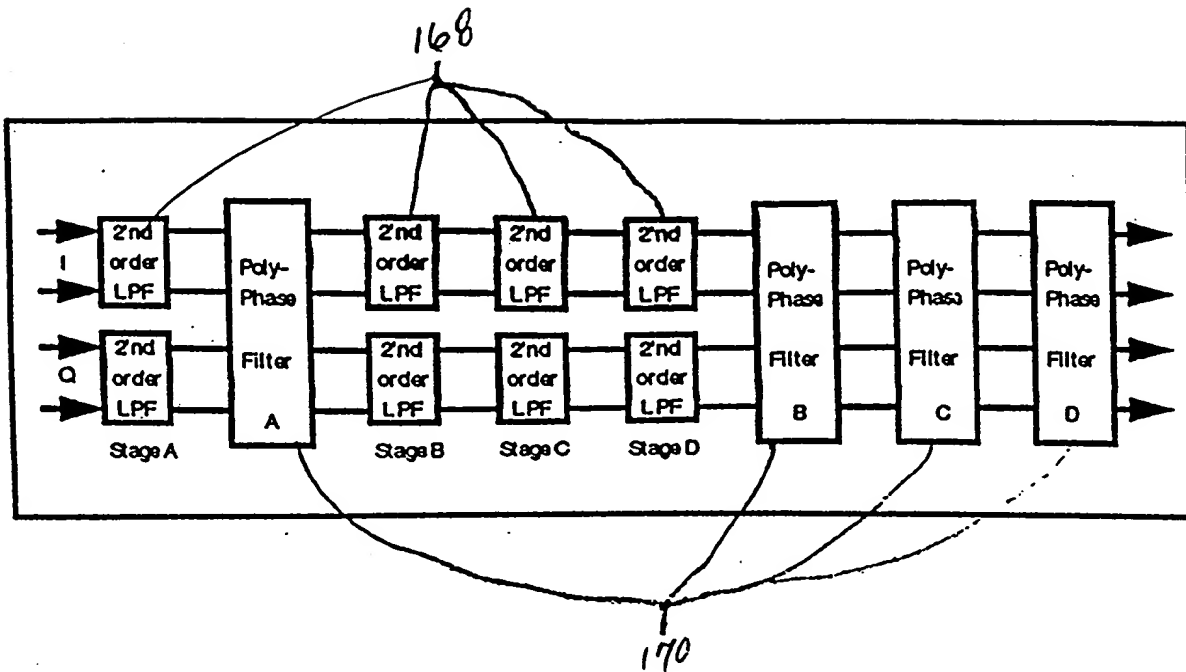


FIG. 13

[illegible]

FIG. 14



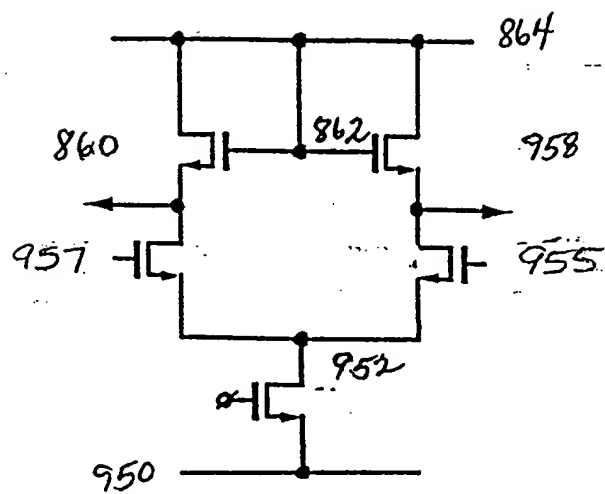


FIG. 16(a)





FIG. 17(a)

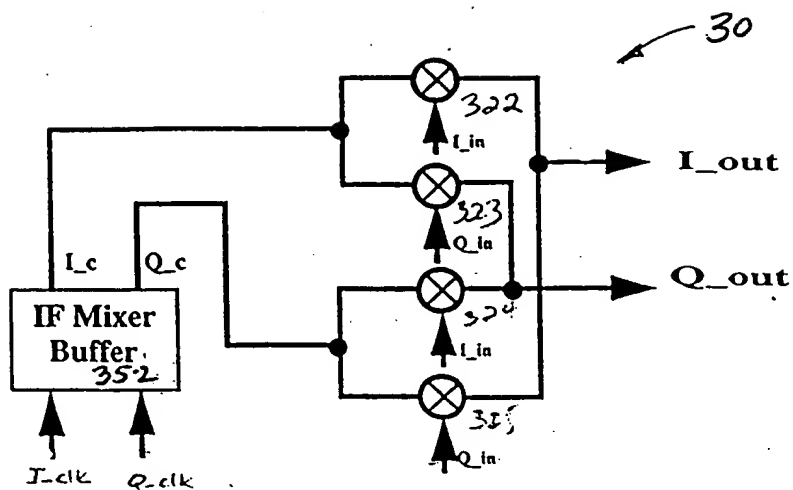


FIG. 17(b)

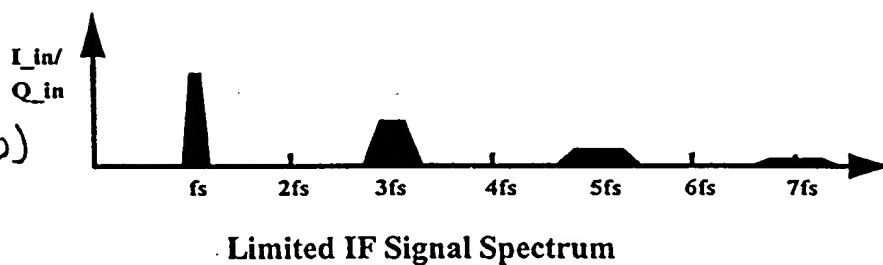


FIG. 17(c)

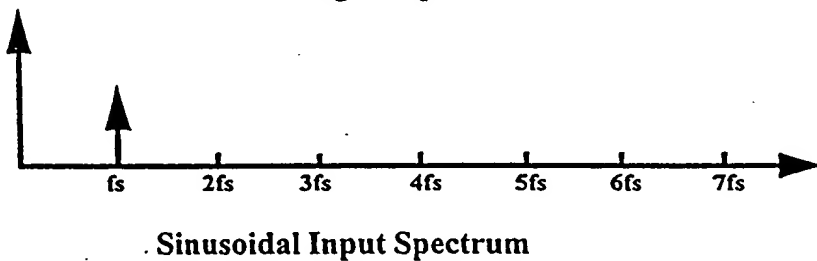


FIG. 17(d)

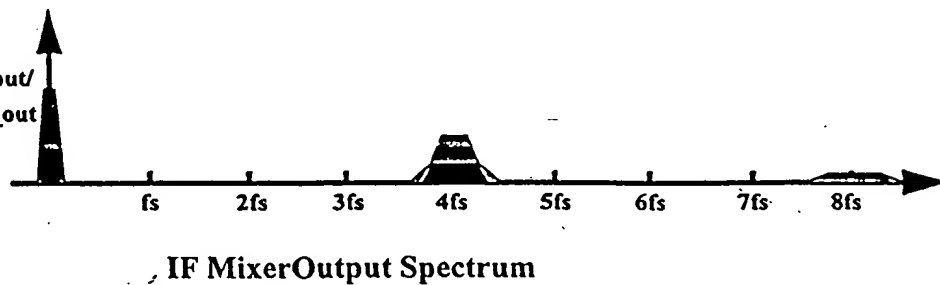


FIG. 18

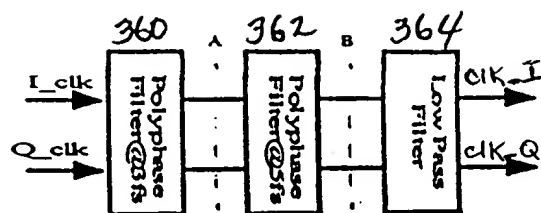


FIG. 19(a)

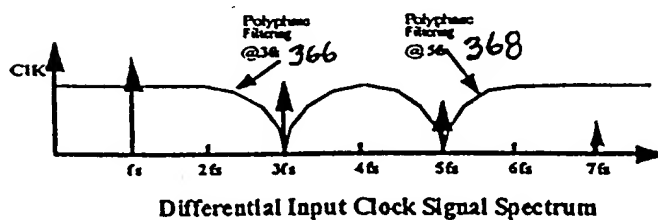


FIG. 19(b)

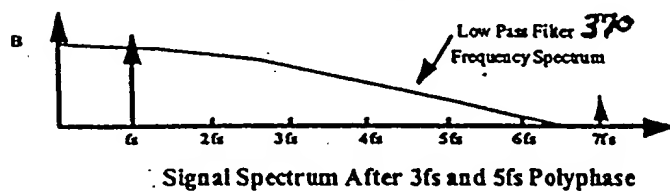
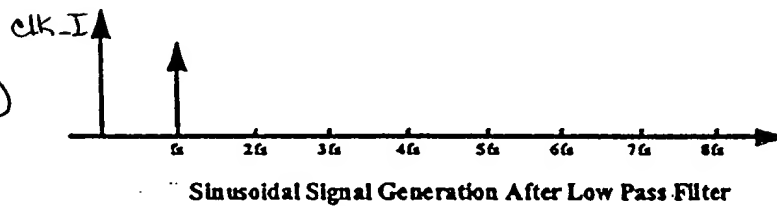


FIG. 19(c)



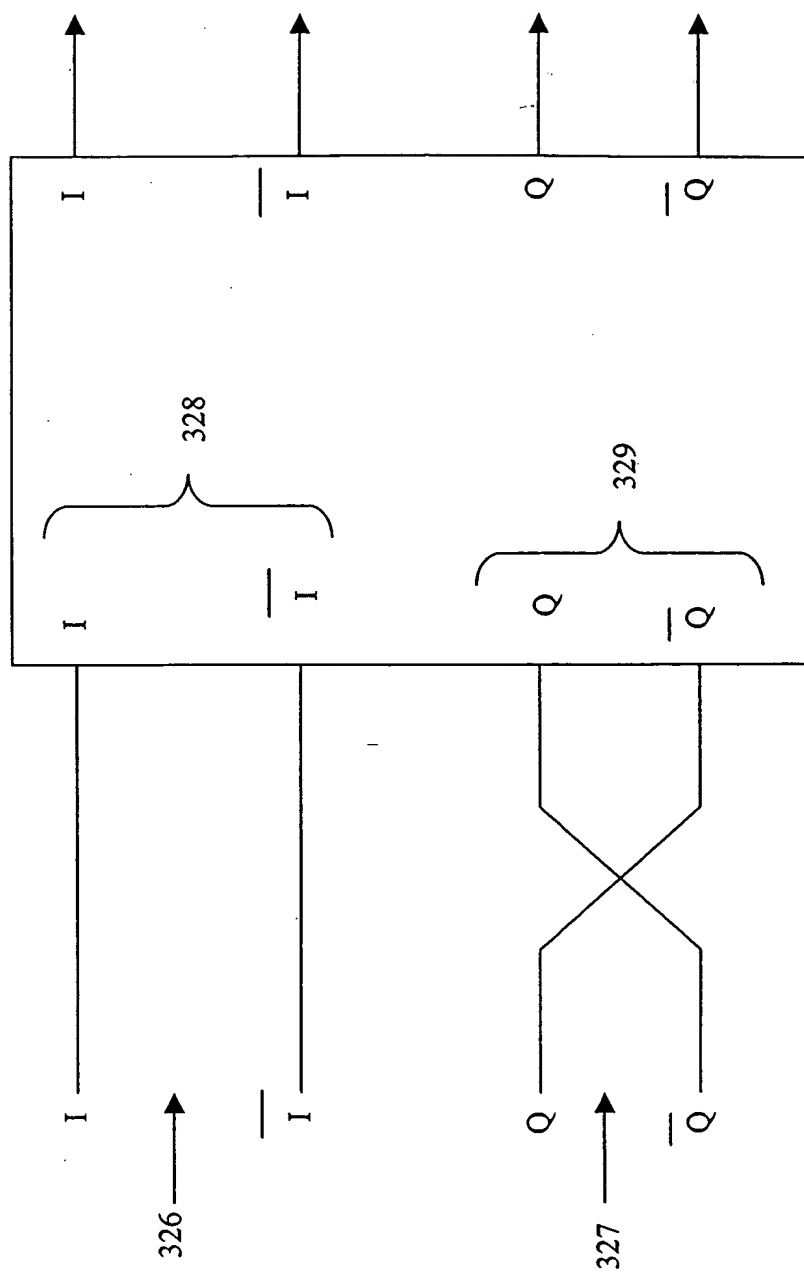


FIG. 19d

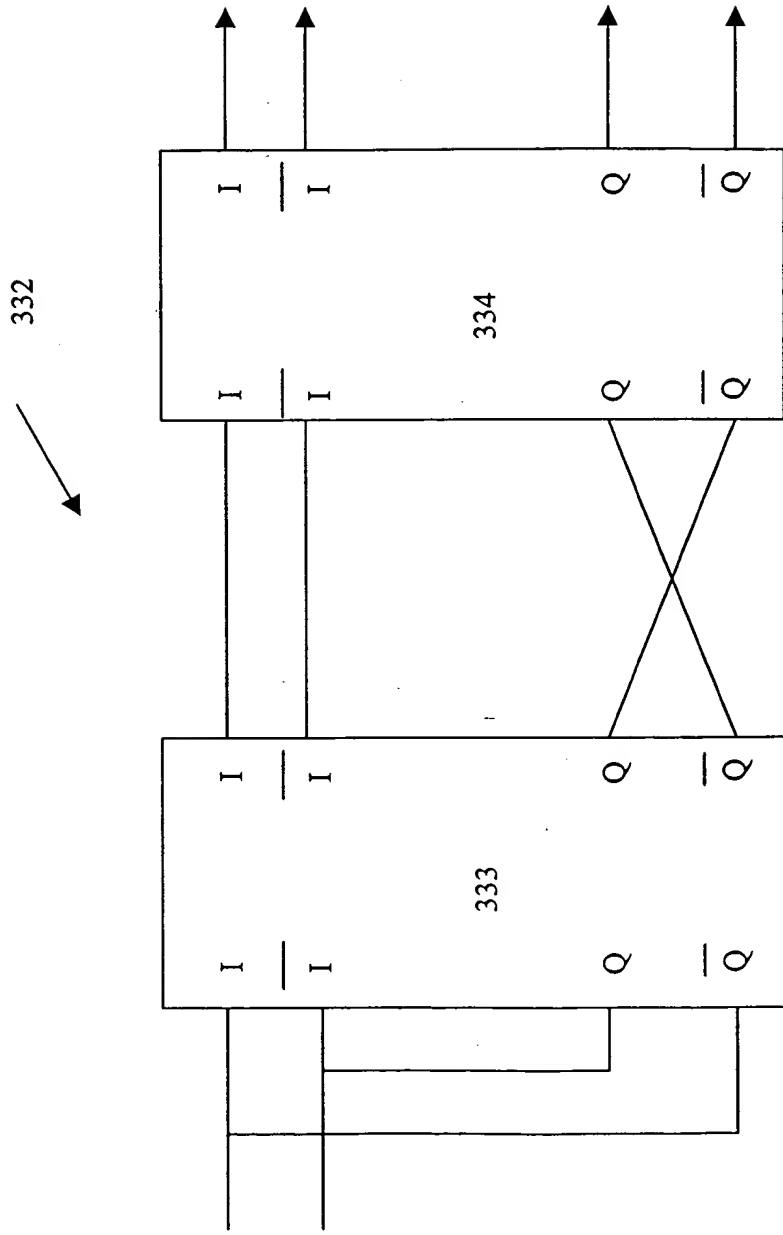


FIG. 19e

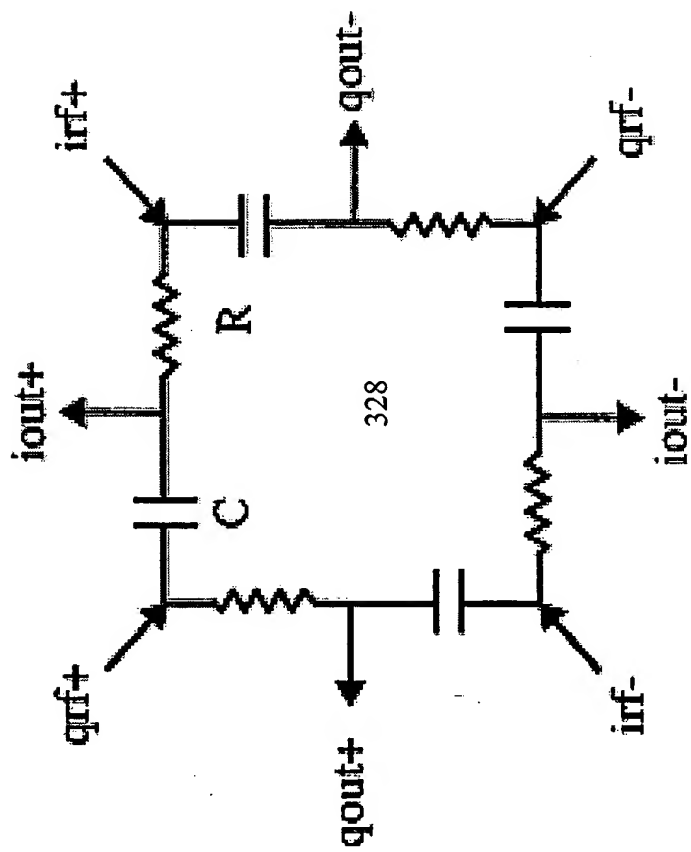
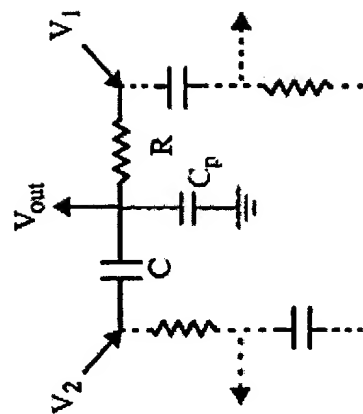


FIG. 19f



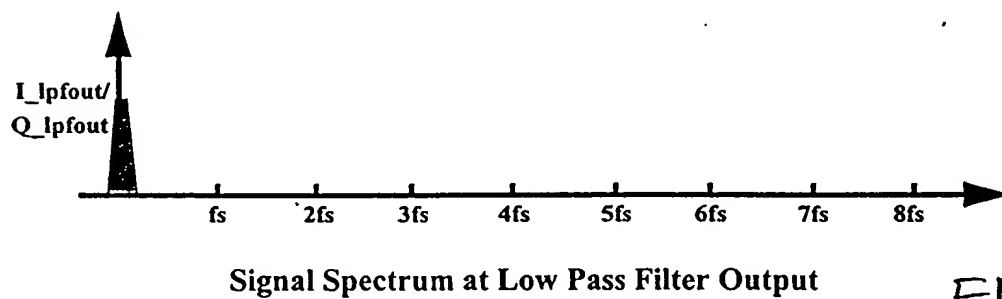
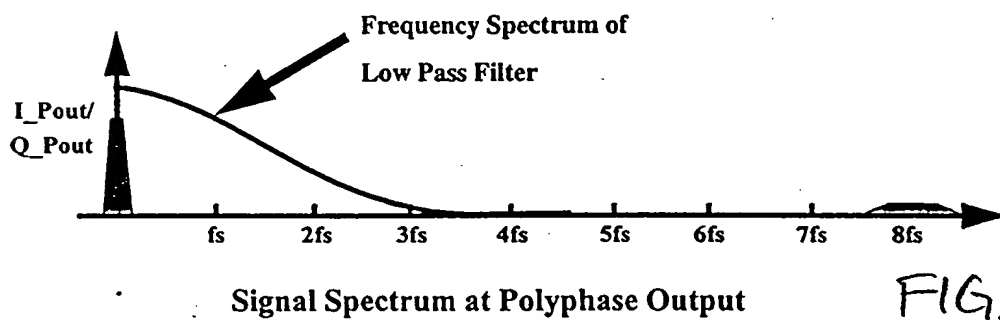
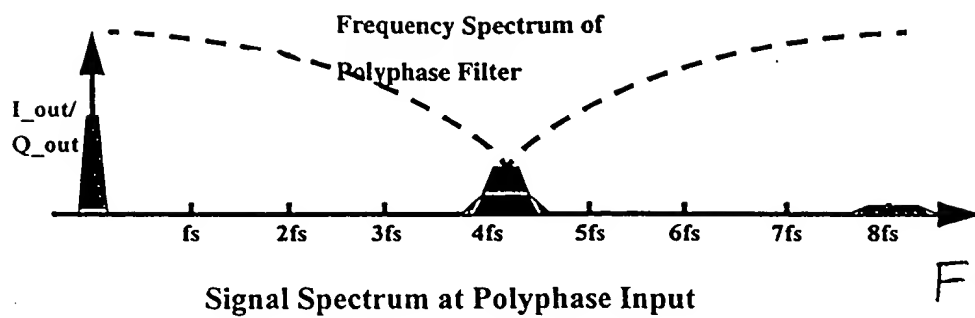
$$\omega_p = \frac{1}{R(C_p + C)}$$

$$\omega_o = \frac{1}{RC}$$

$$V_{out} = \frac{V_1}{R(C_p + C)s + 1} + \frac{V_2 RCs}{R(C_p + C)s + 1}$$



FIG. 19g





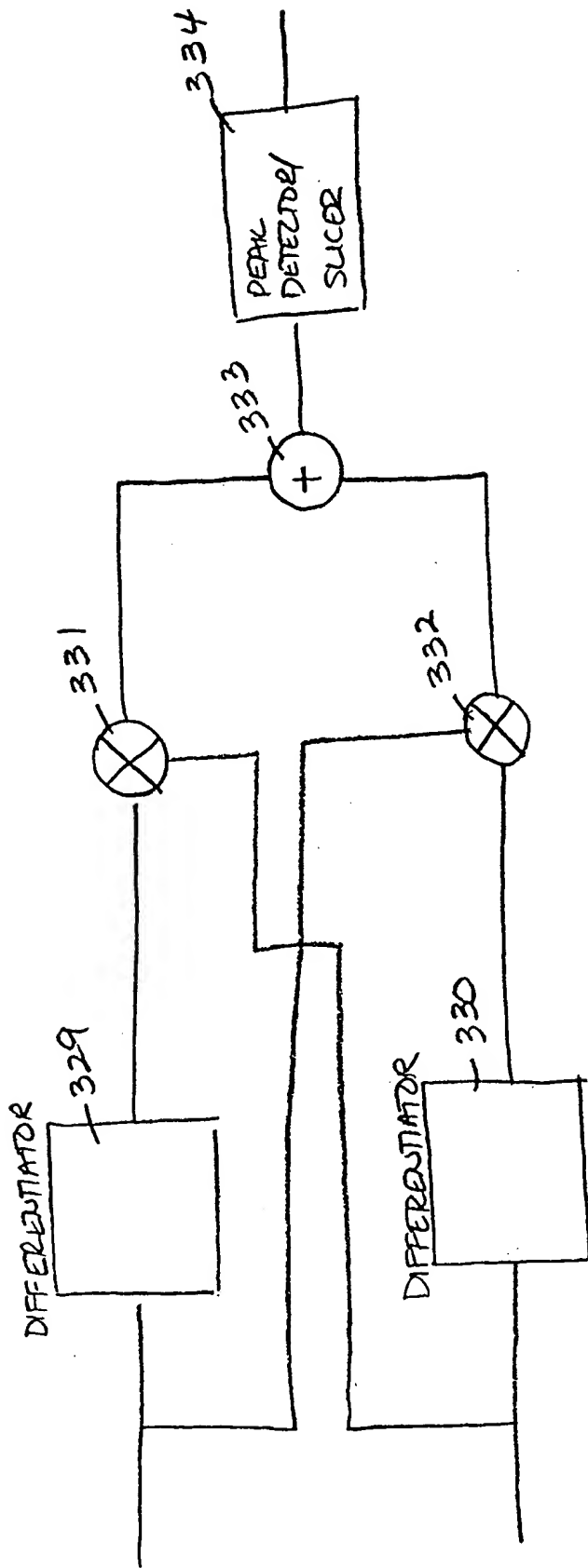


FIG. 21

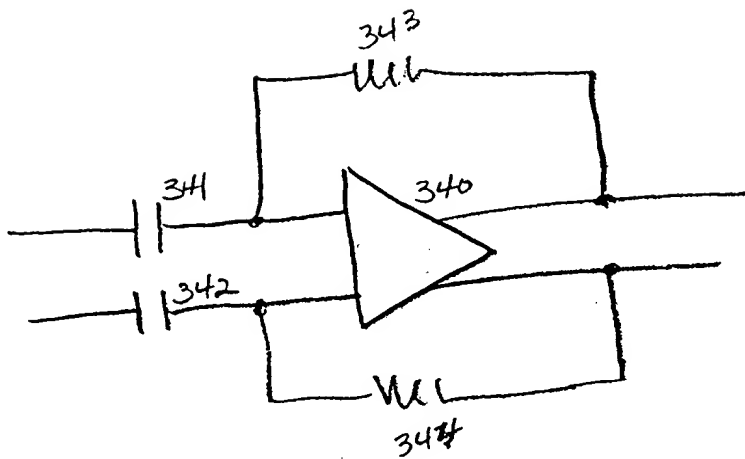


FIGURE 22

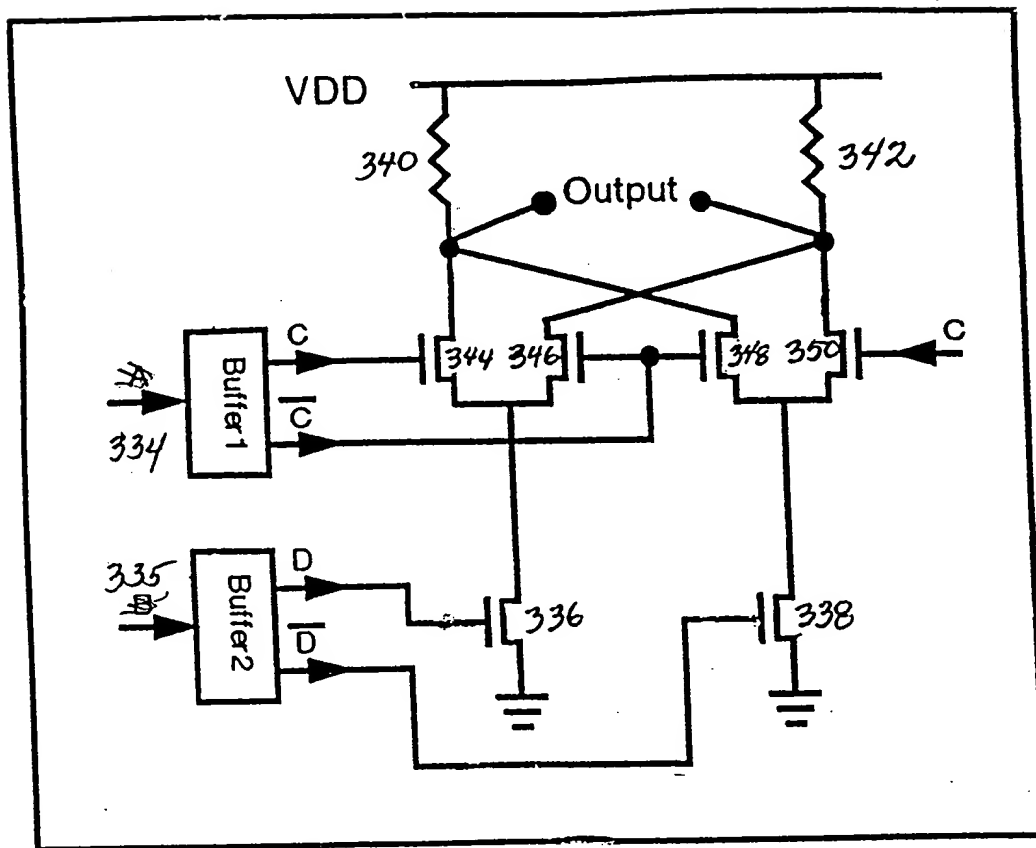


FIG. 23

1. The circuit is a schematic diagram of a signal processing system.

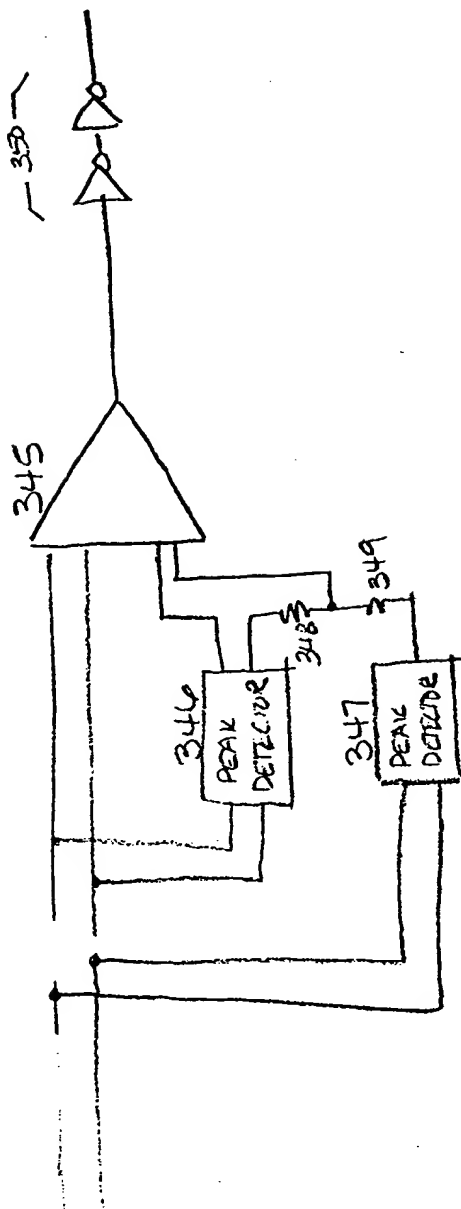


FIGURE 24



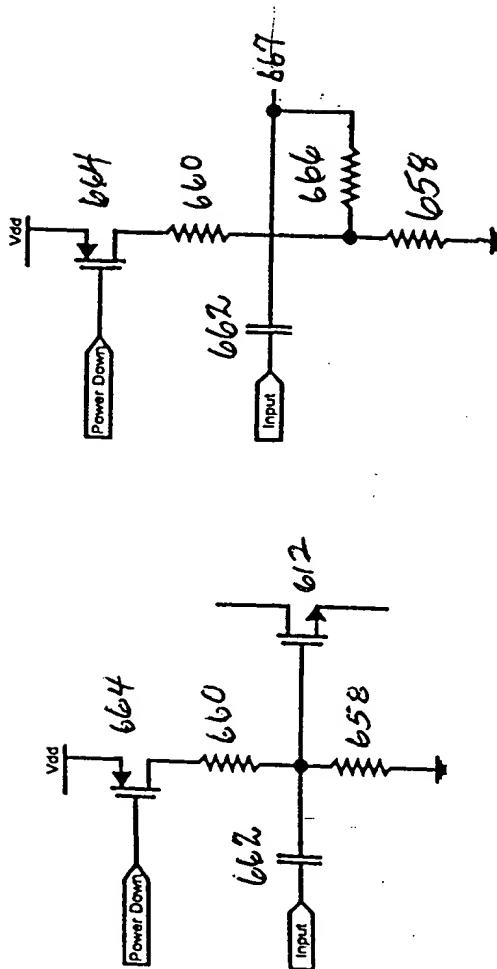


FIG. 26(a)

FIG. 26(b)

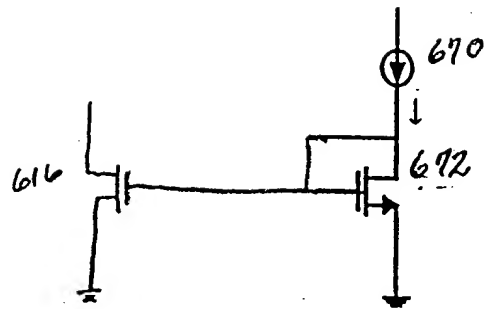


FIG. 27





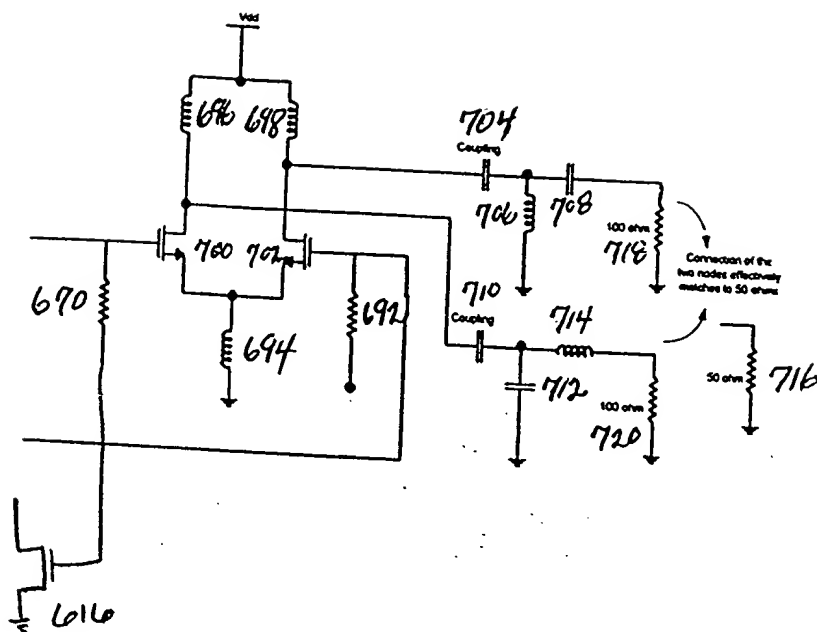


FIG. 29



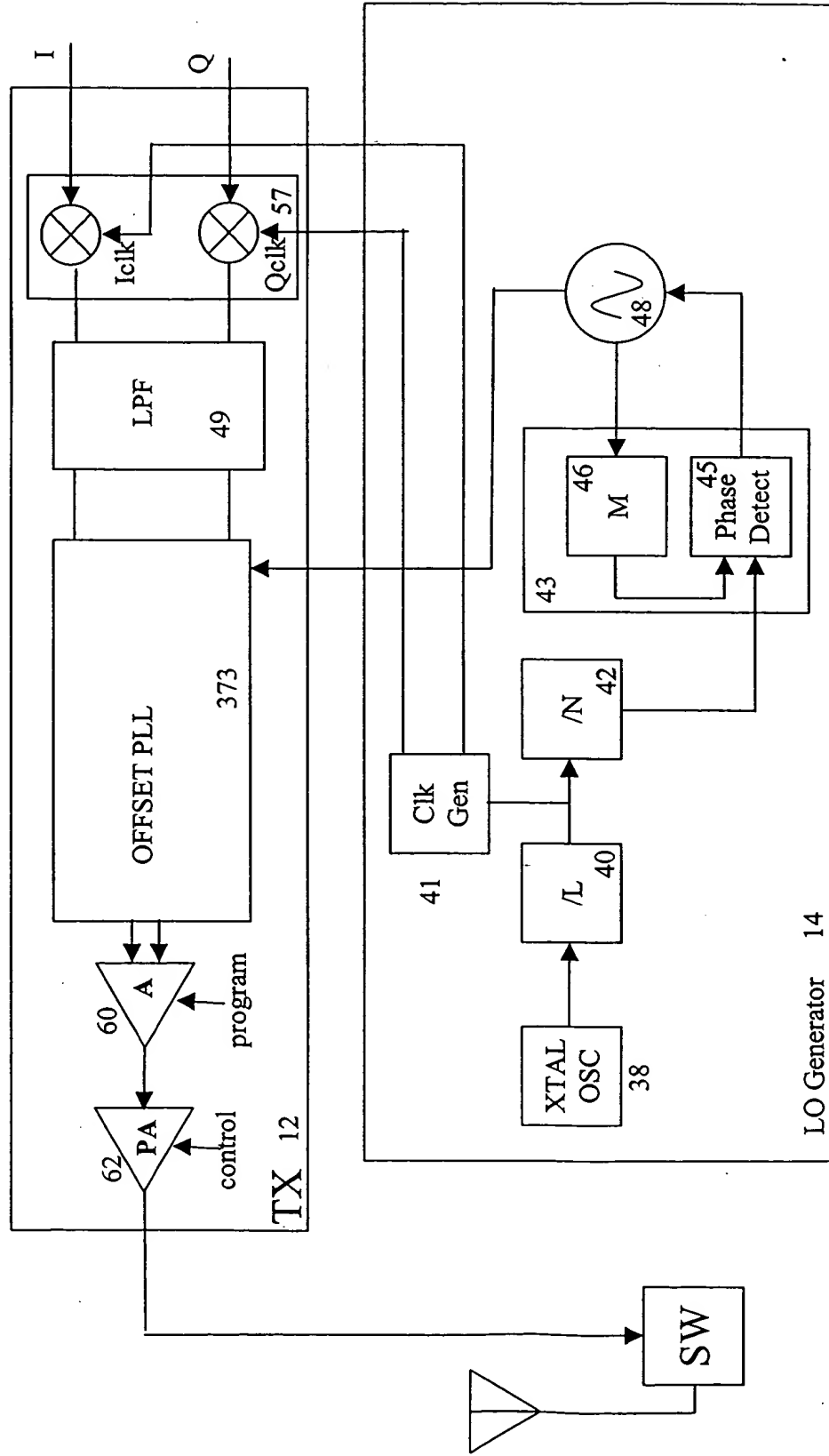


FIG. 30b

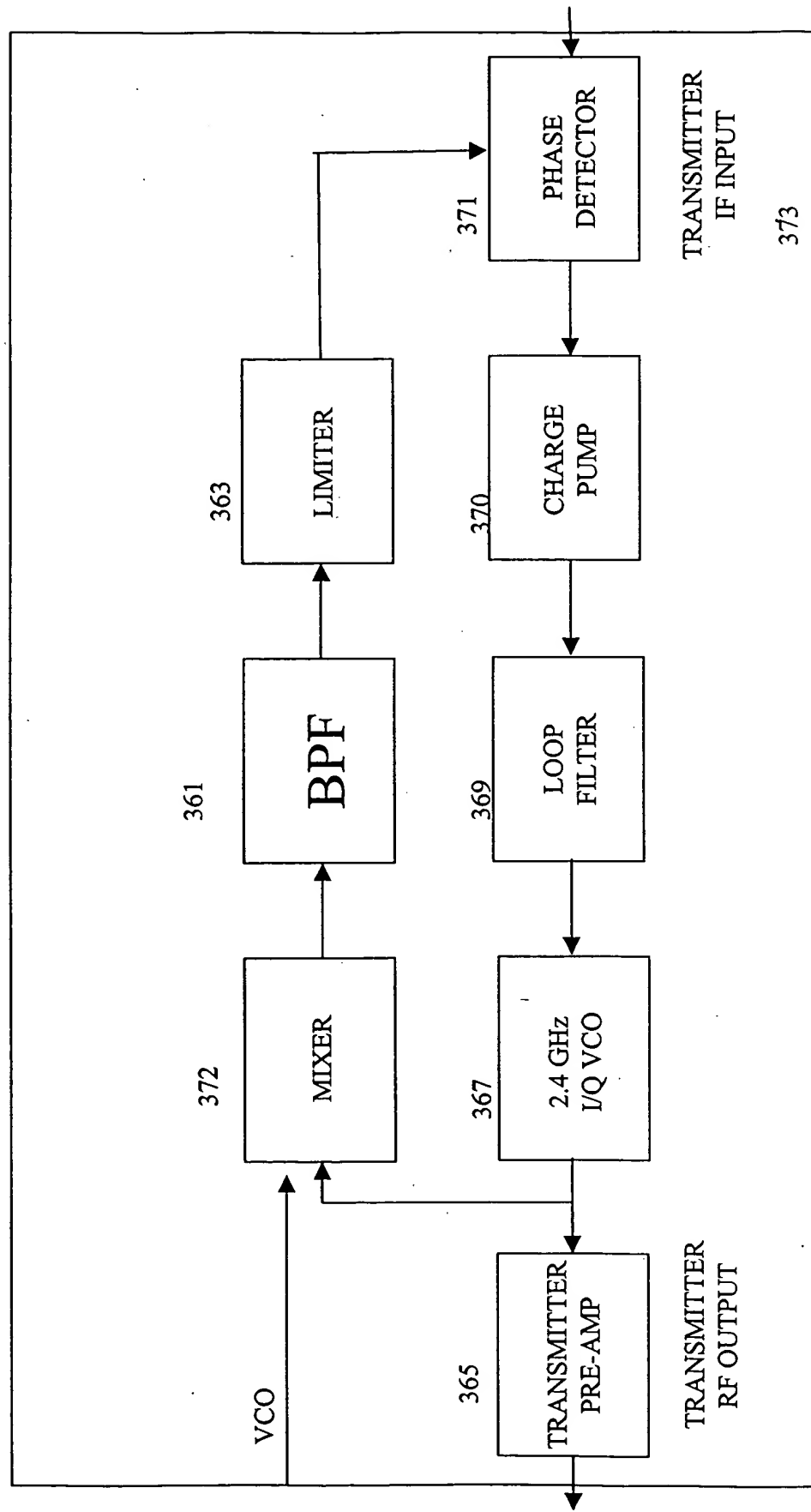


FIG. 30c

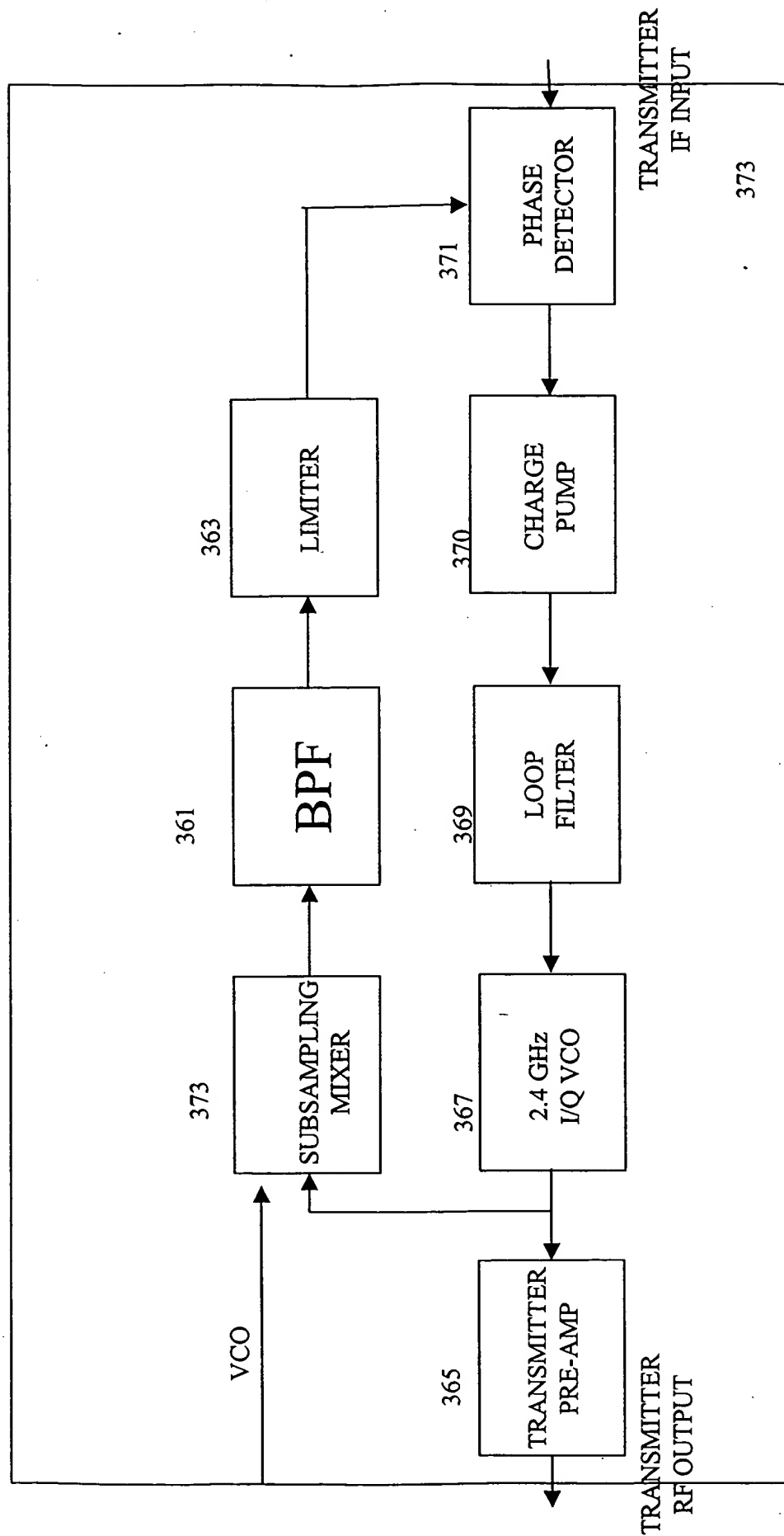


FIG. 30d

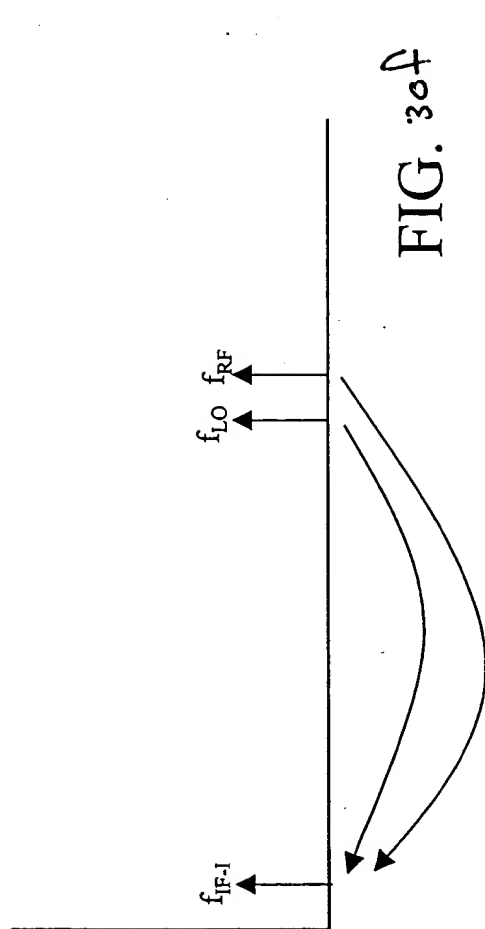


FIG. 30d

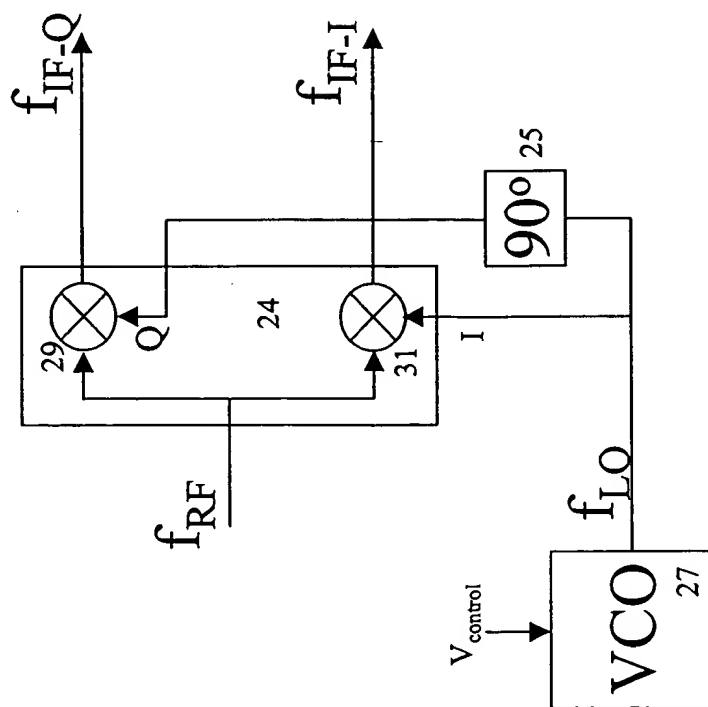


FIG. 30e

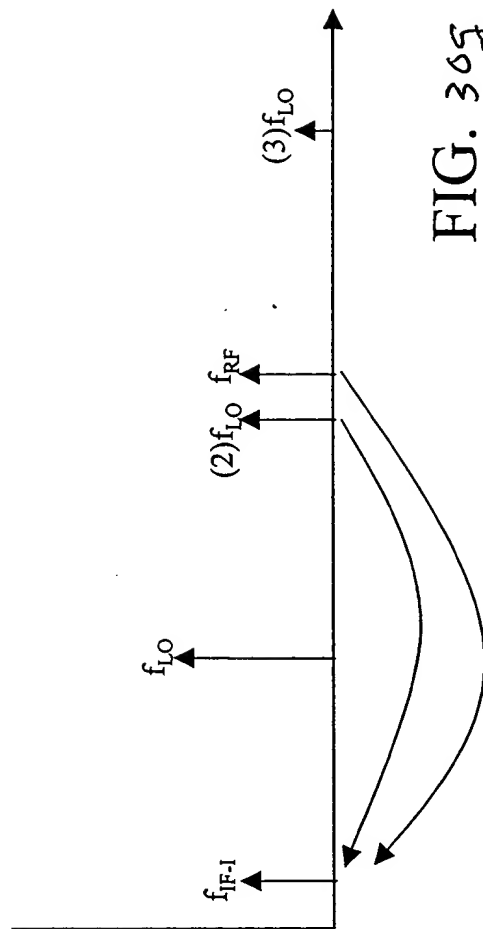


FIG. 30f

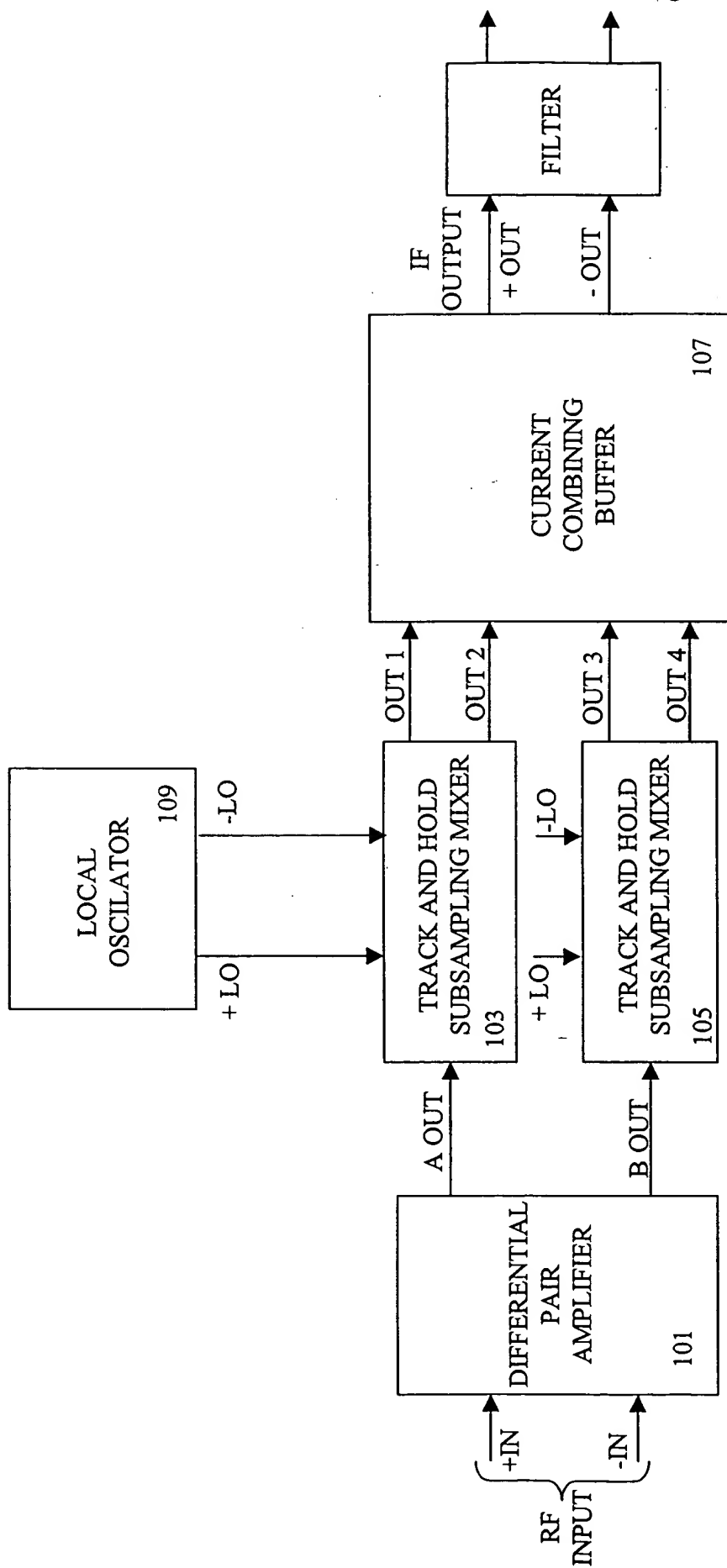


FIG. 30k

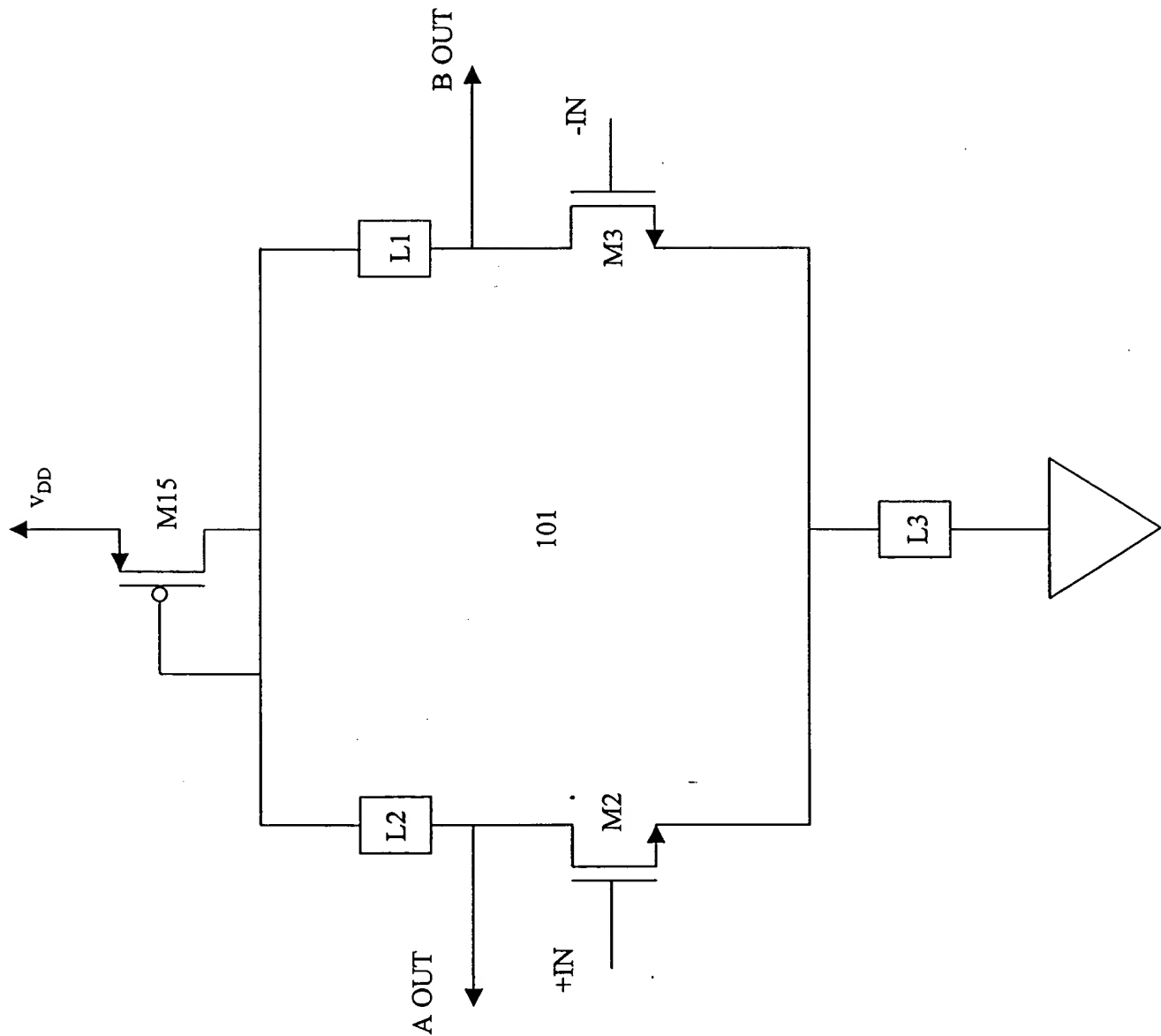


FIG. 30λ



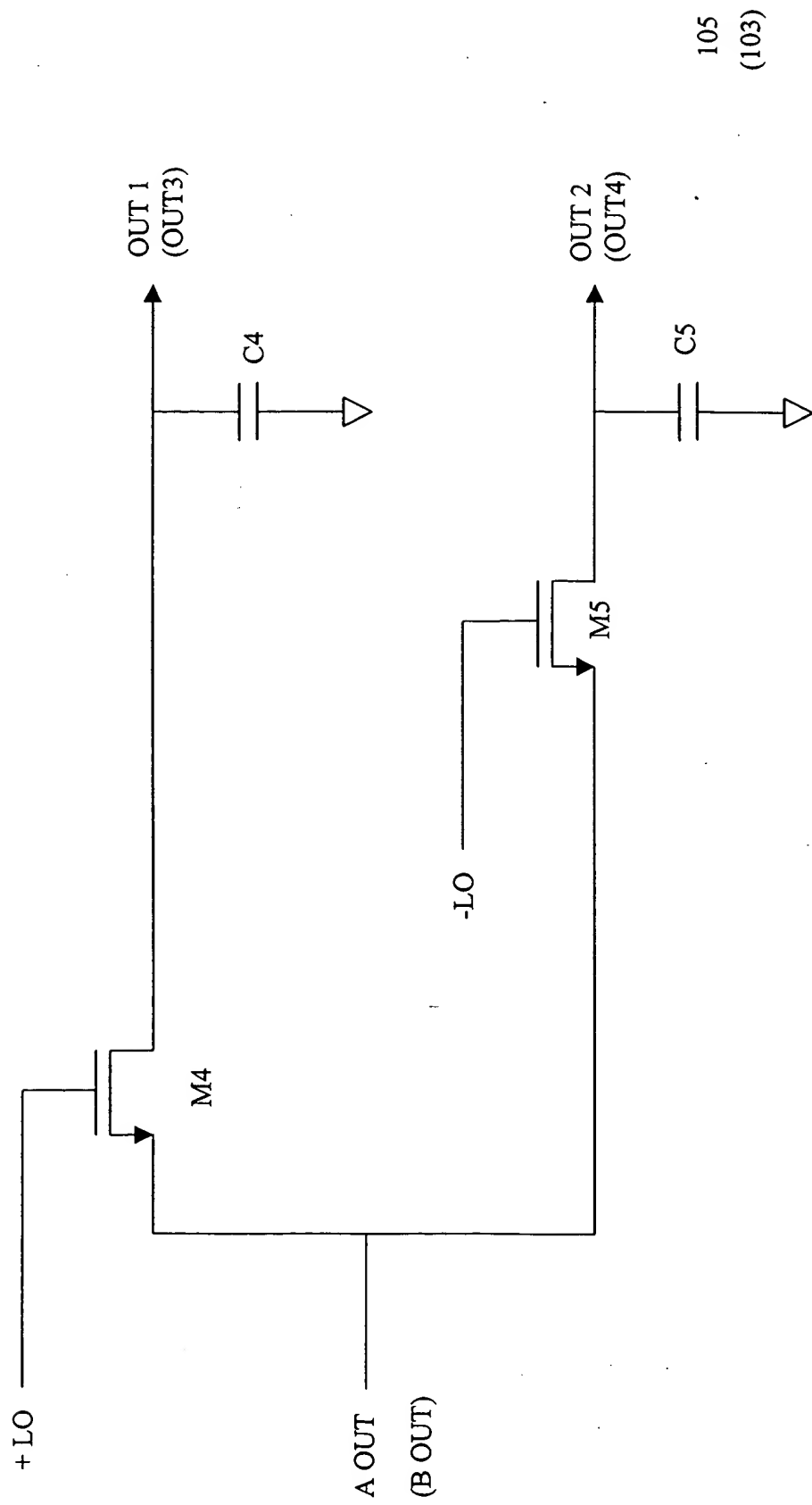


FIG. 30j

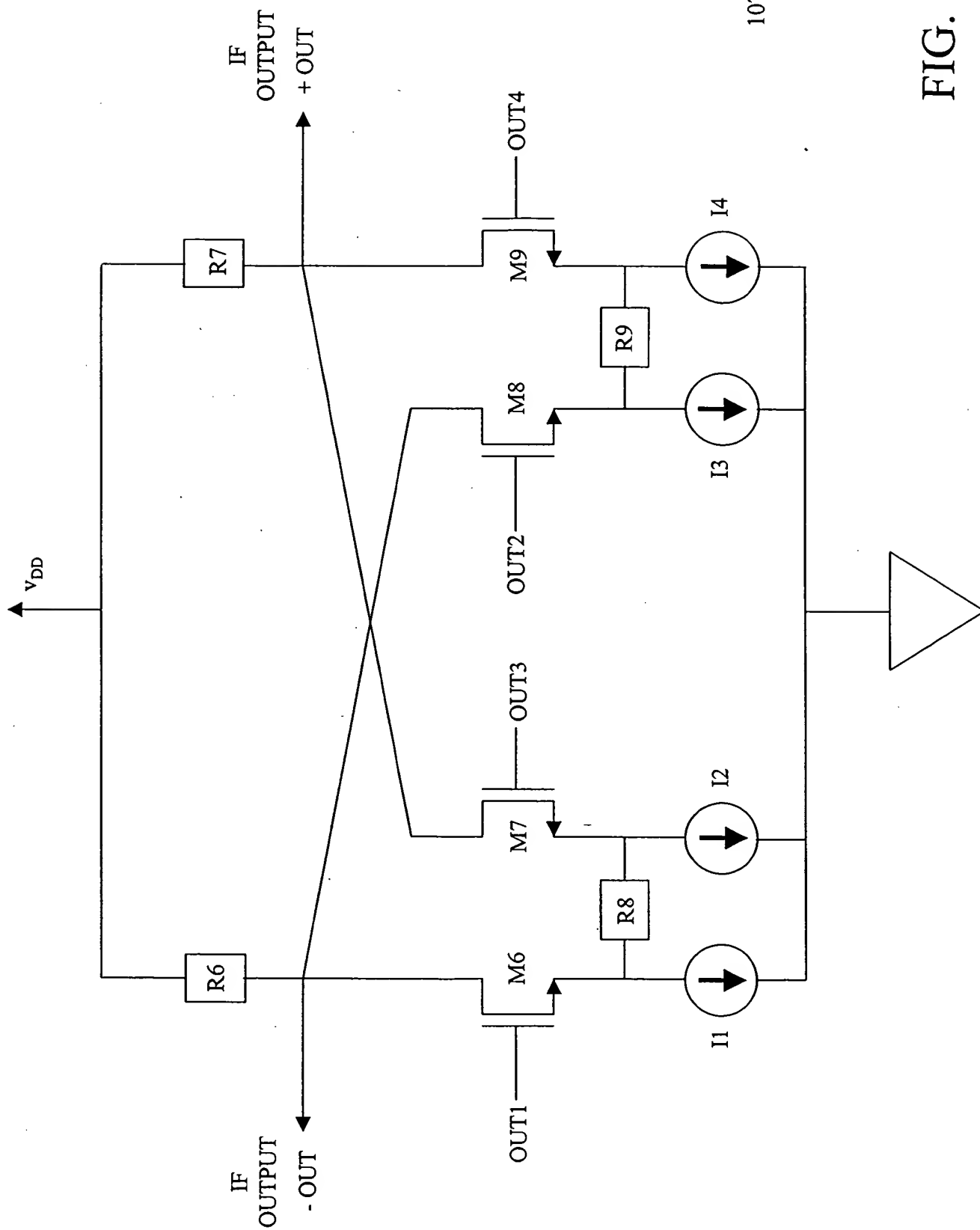
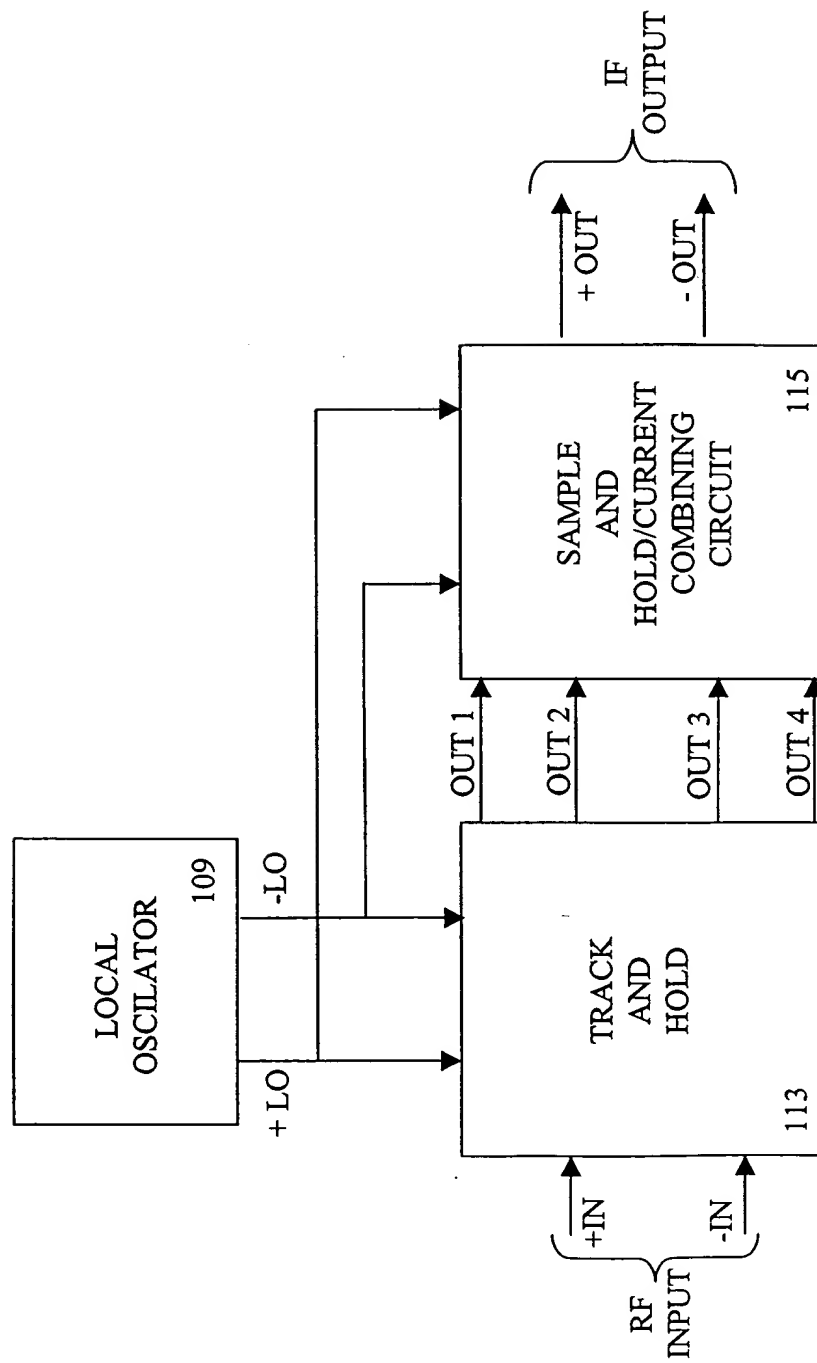
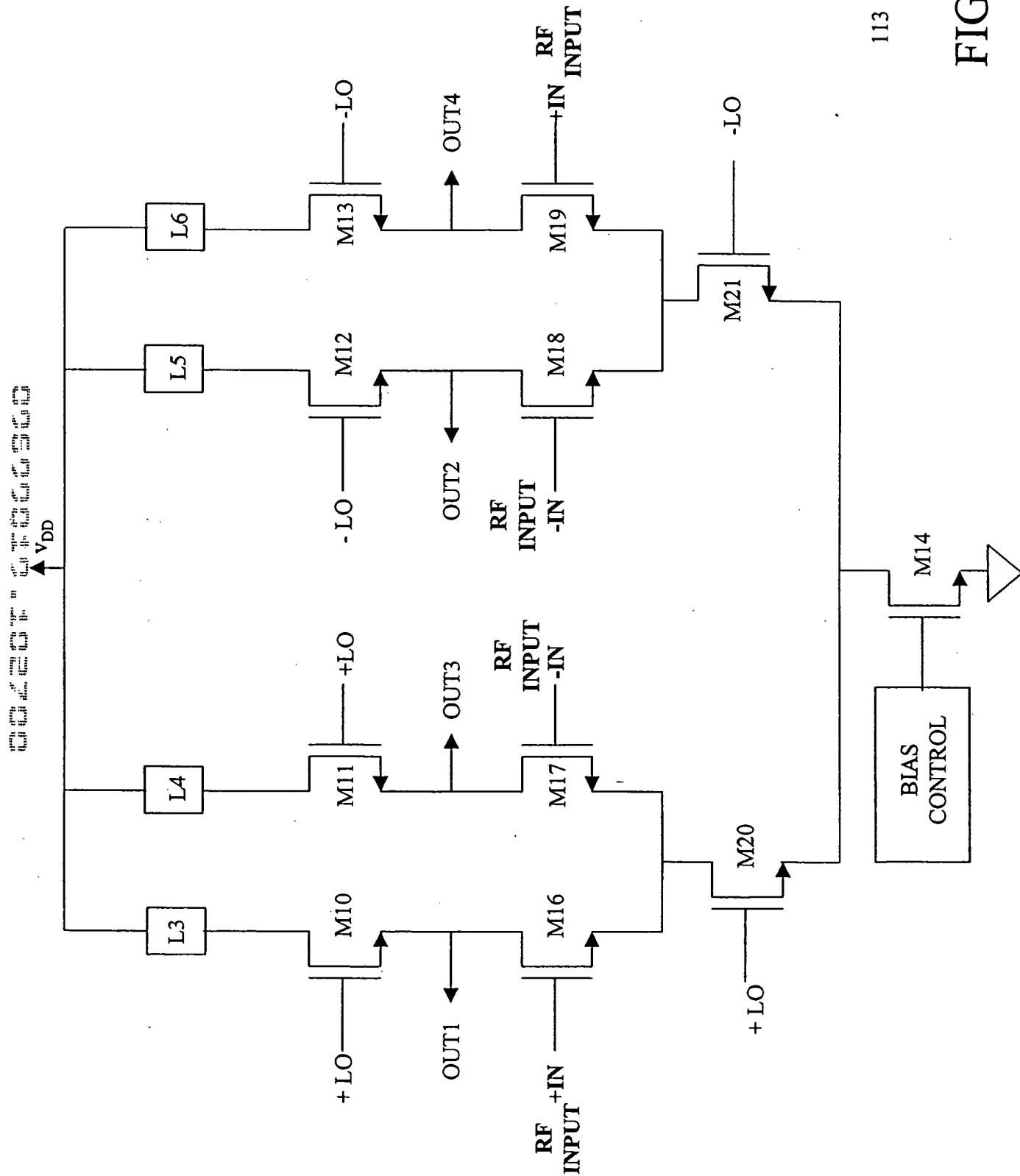


FIG. 30k



111

FIG. 30L



113

FIG. 30m

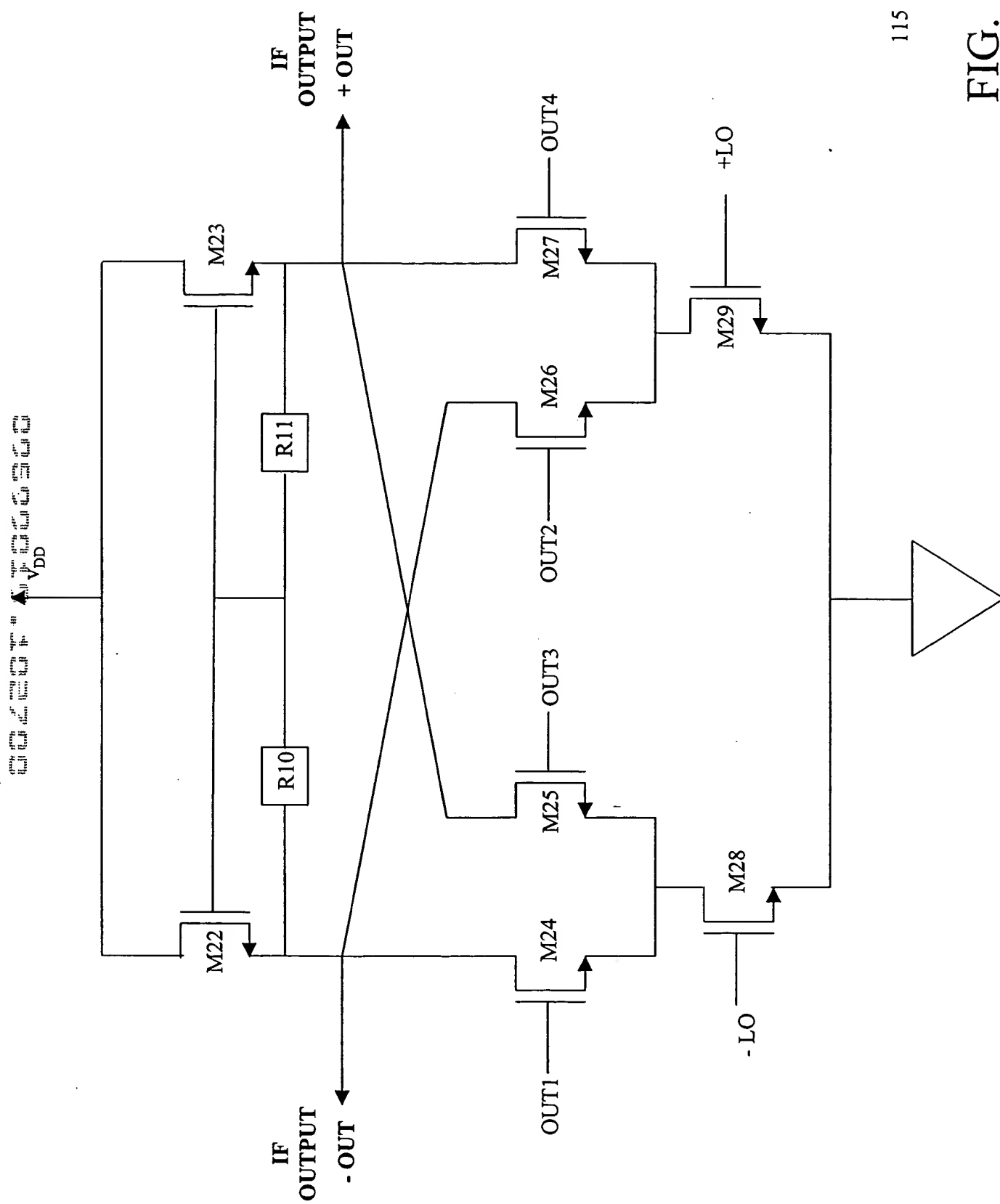


FIG. 30N

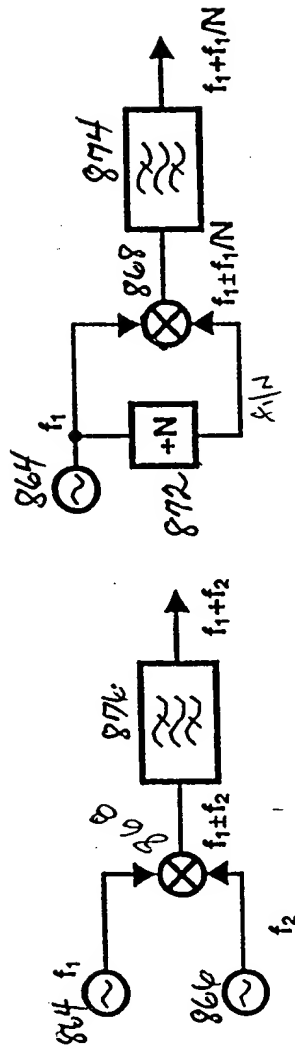


FIG. 31(a)

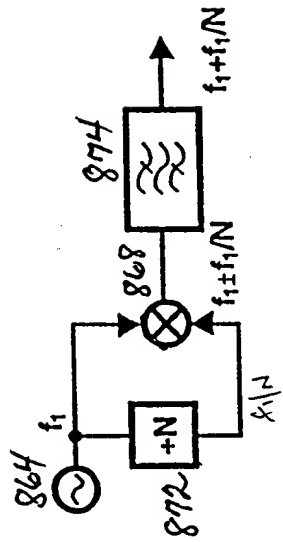


FIG. 31(b)

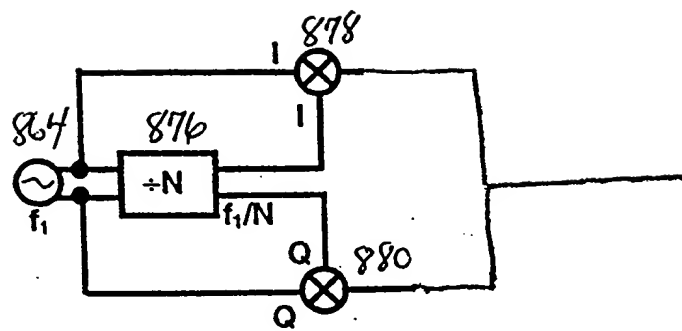


FIG. 32

1. The circuit is a differential amplifier with two input channels, labeled  $f_{1,1}$  and  $f_{1,2}$ .  
 2. The input channels are connected to a common input signal  $f_{1,1}$  and  $f_{1,2}$ .  
 3. The output channels are connected to a common output signal  $f_{1,1}$  and  $f_{1,2}$ .  
 4. The circuit includes a feedback loop with a gain of  $-1$ .  
 5. The circuit is designed to amplify the input signal by a factor of  $10$ .  
 6. The circuit is a differential amplifier with two input channels, labeled  $f_{1,1}$  and  $f_{1,2}$ .  
 7. The input channels are connected to a common input signal  $f_{1,1}$  and  $f_{1,2}$ .  
 8. The output channels are connected to a common output signal  $f_{1,1}$  and  $f_{1,2}$ .  
 9. The circuit includes a feedback loop with a gain of  $-1$ .  
 10. The circuit is designed to amplify the input signal by a factor of  $10$ .

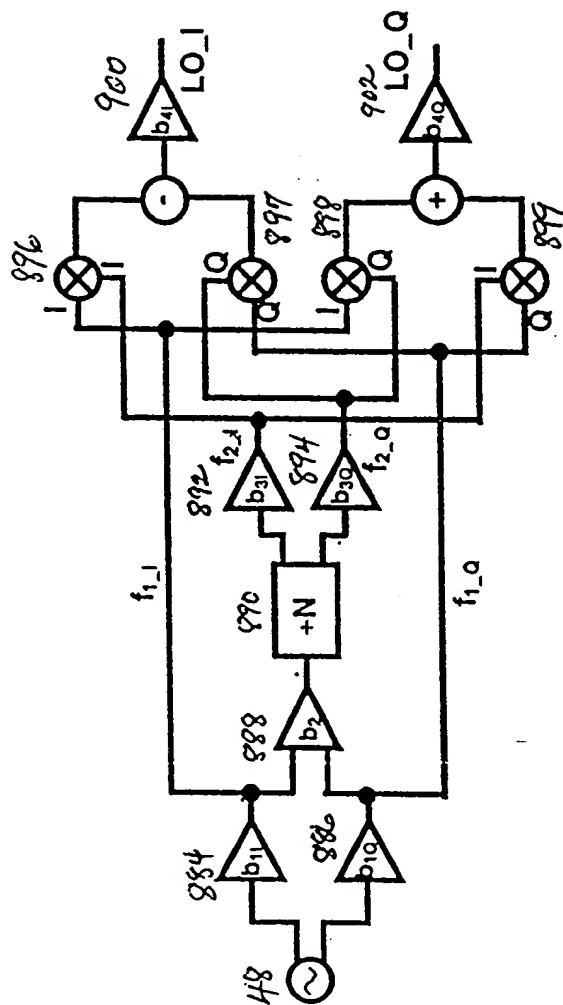


FIG. 33(a)



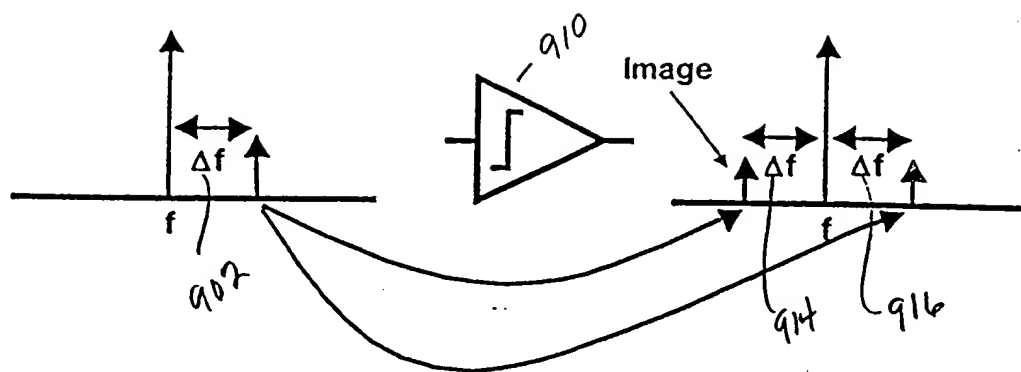


FIG. 33(b)

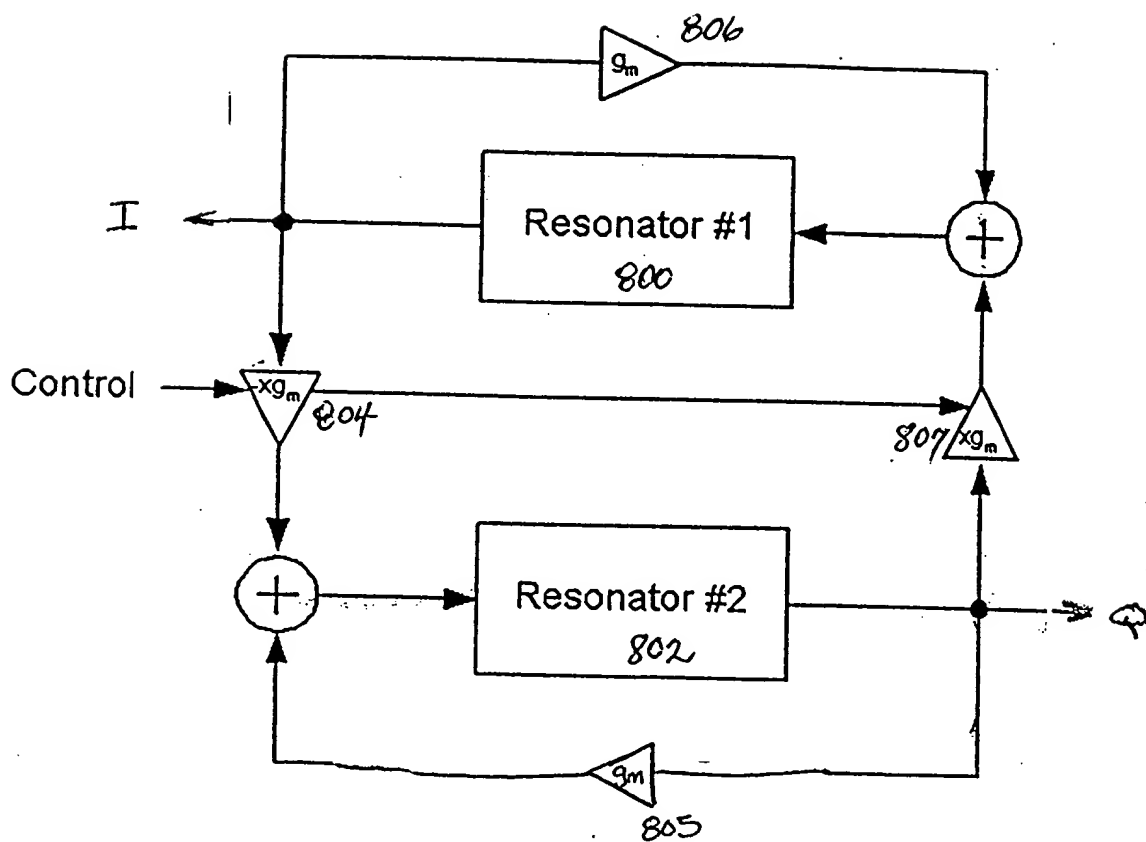


FIG. 34

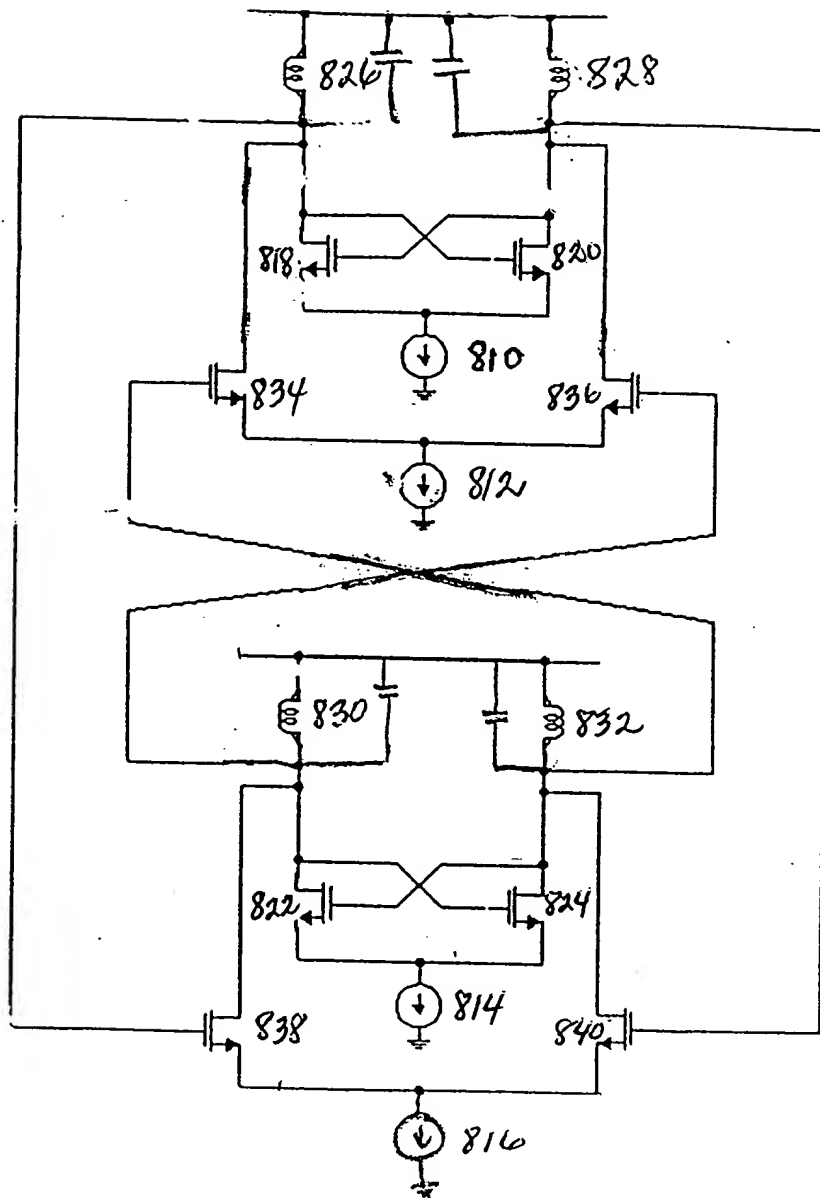


FIG. 35

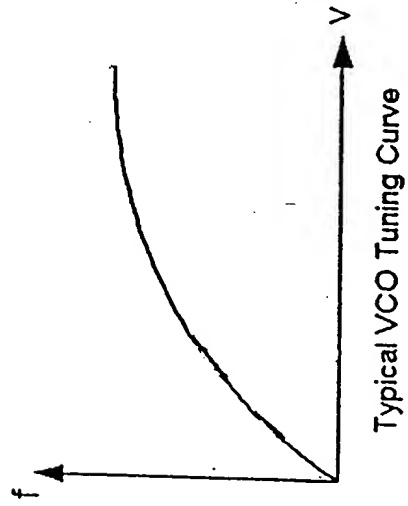


FIG. 36(a)

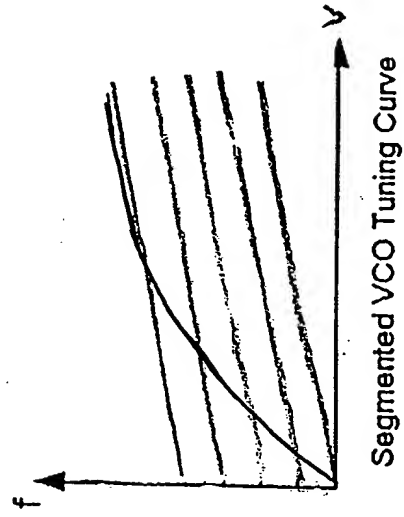


FIG. 36(b)

FIG. 37(a)

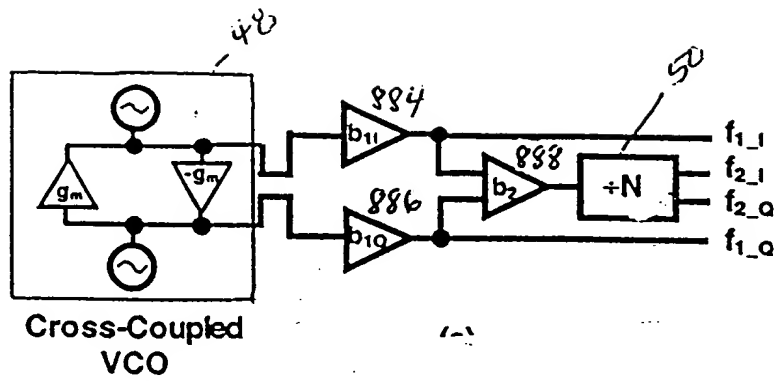
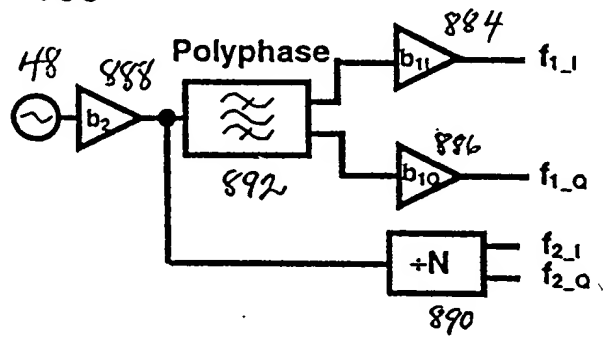


FIG. 37(b)



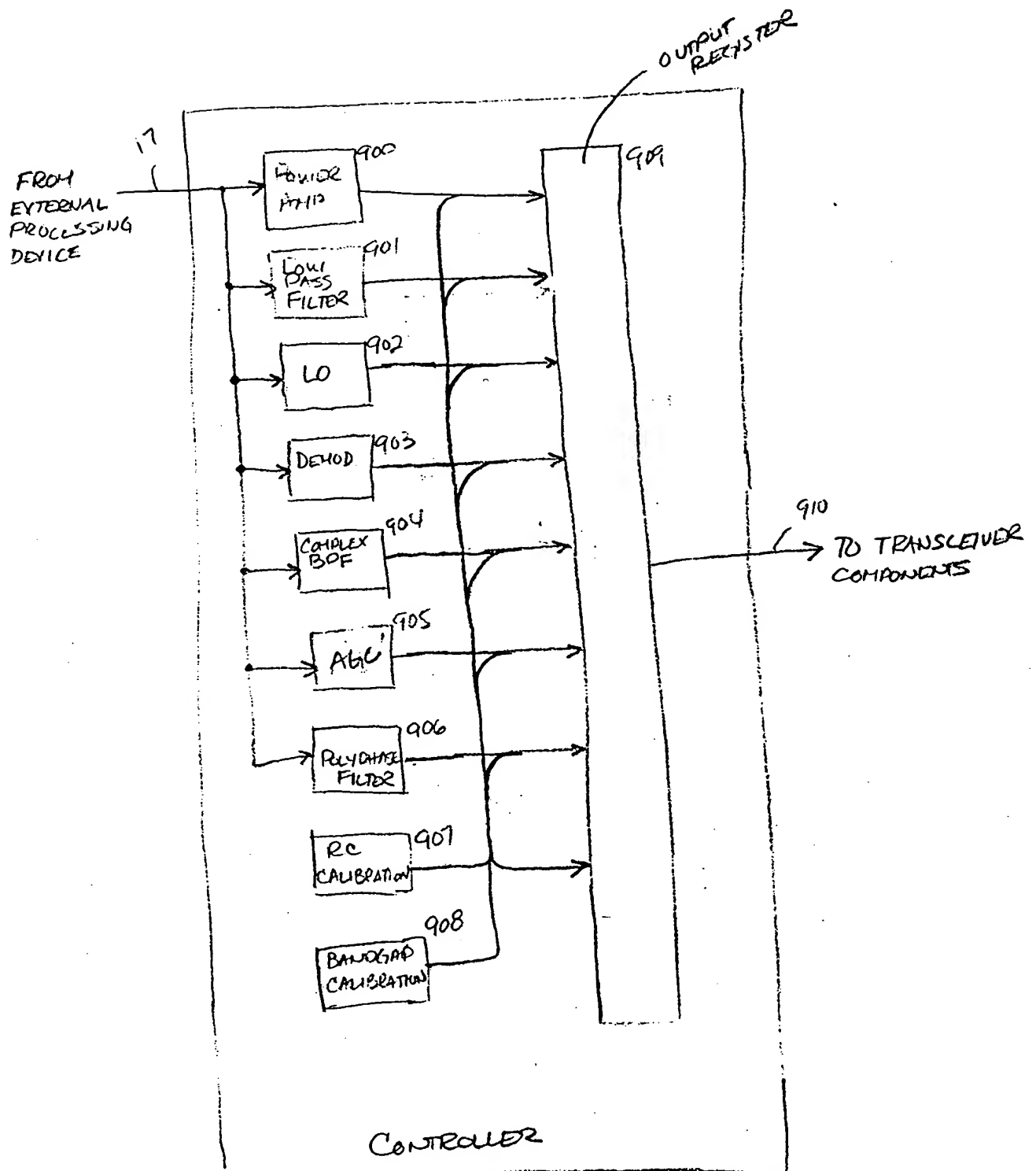


FIGURE 38

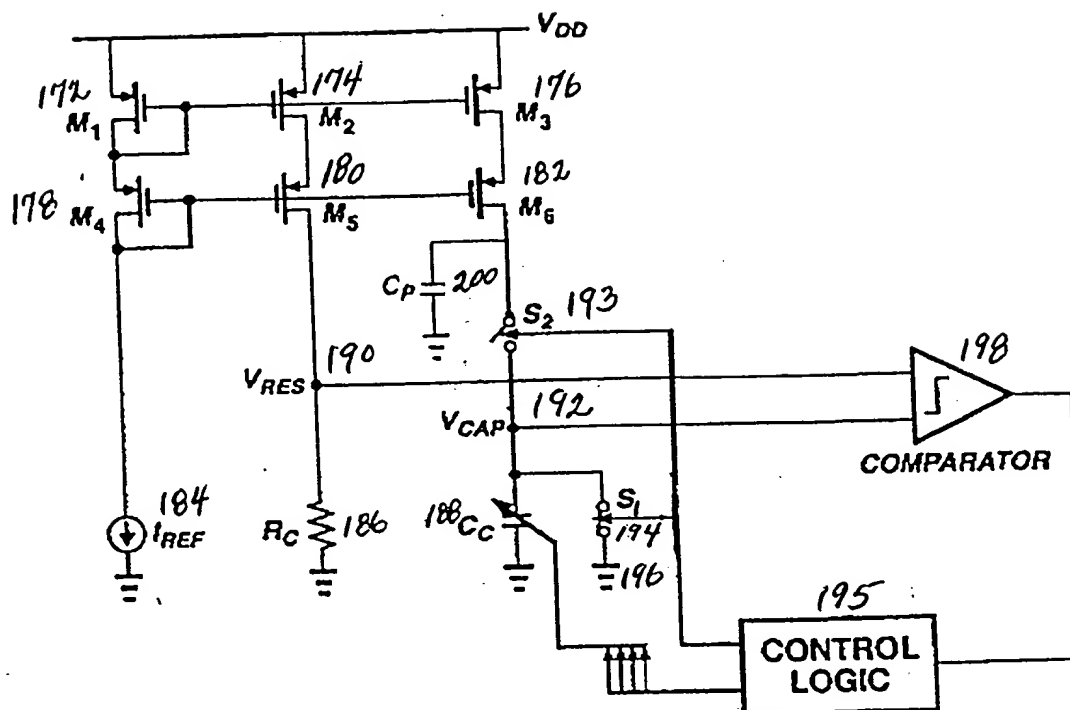


FIG. 39

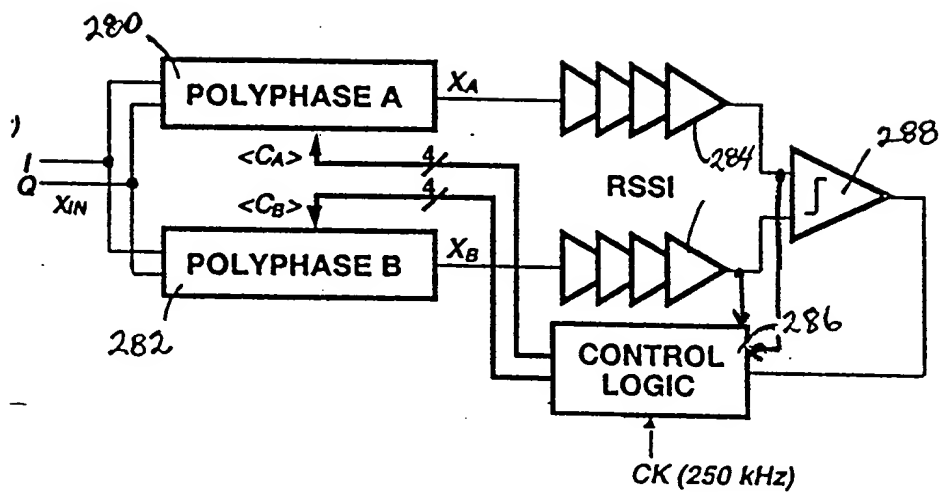


FIG. 40



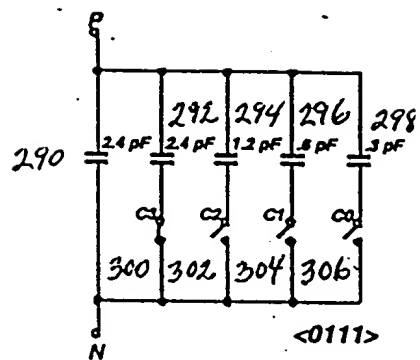


FIG. 41

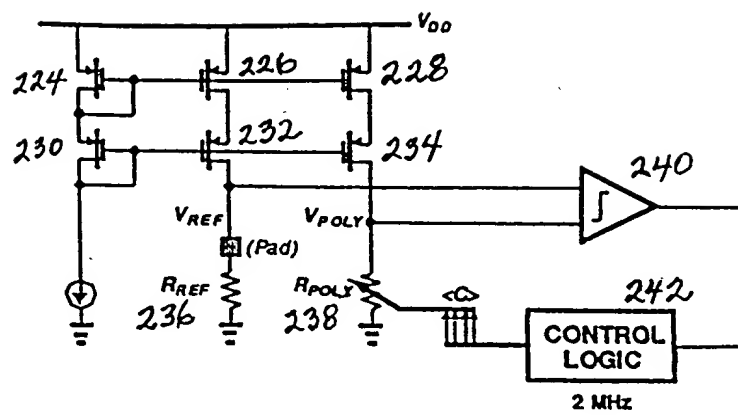


FIG. 42

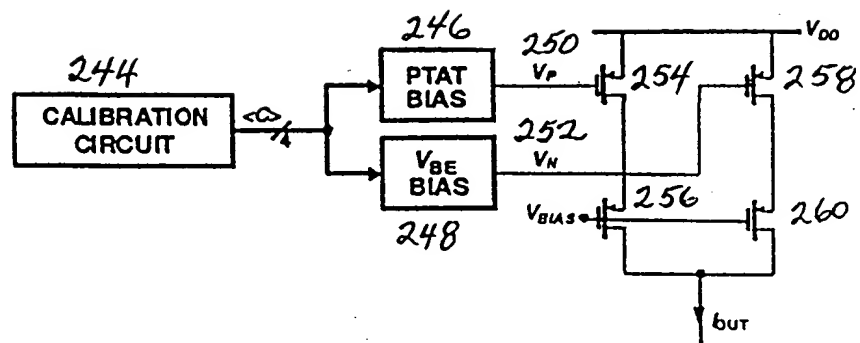


FIG. 43

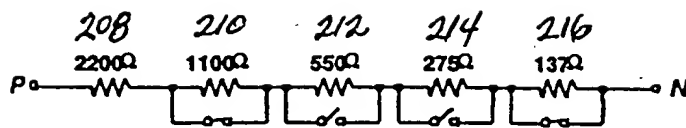


FIG. 44



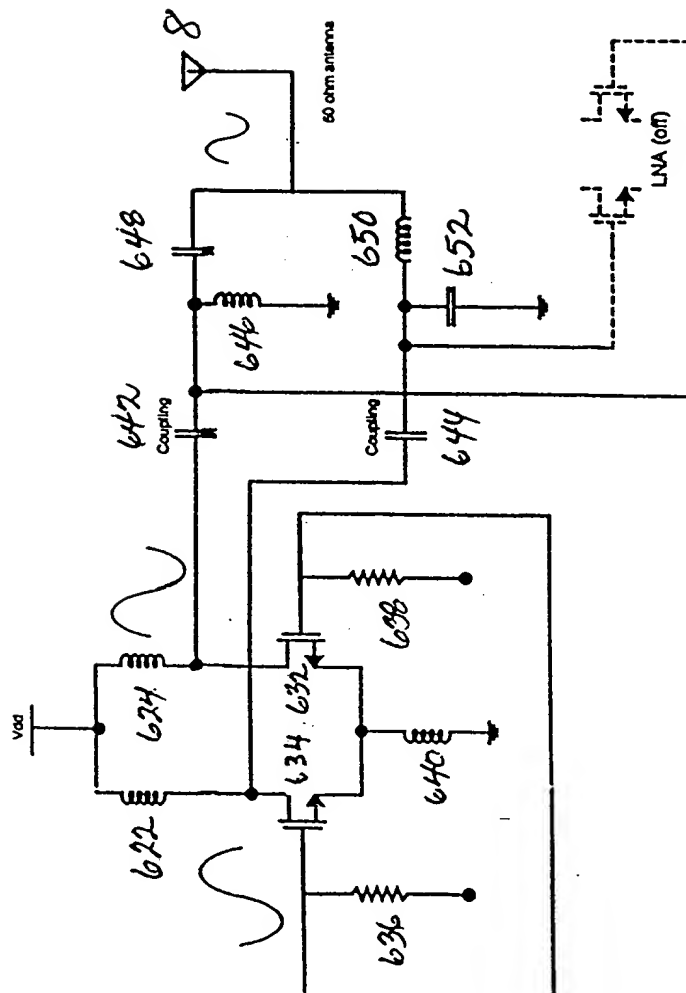


FIG. 46

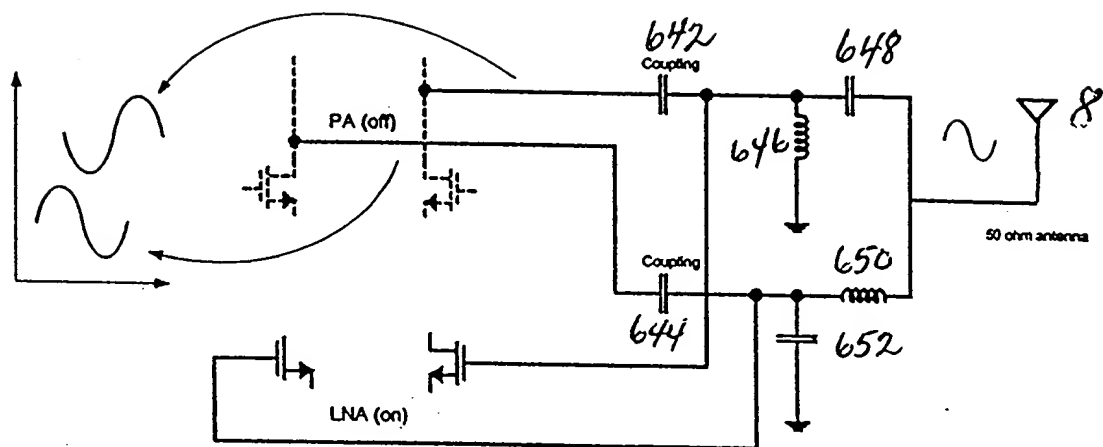


FIG. 47

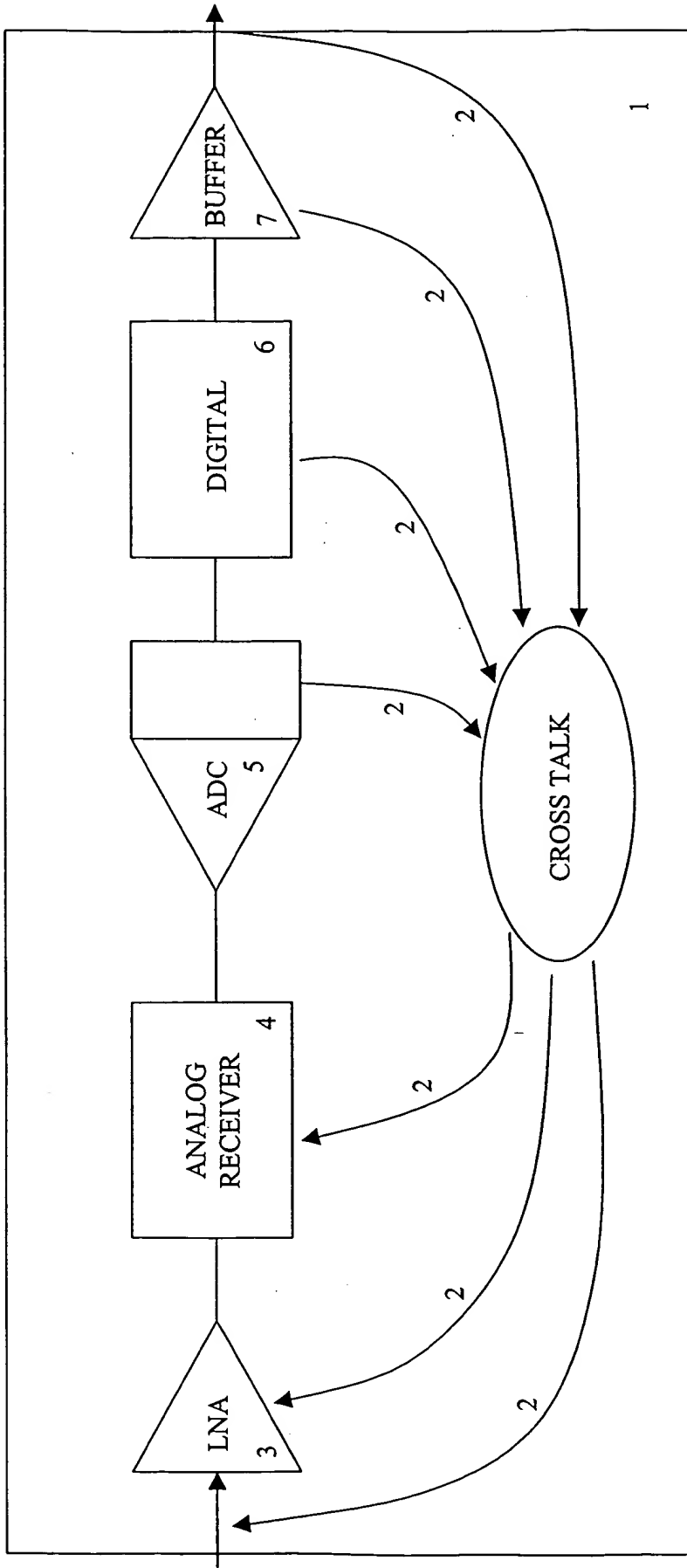


FIG. 48a



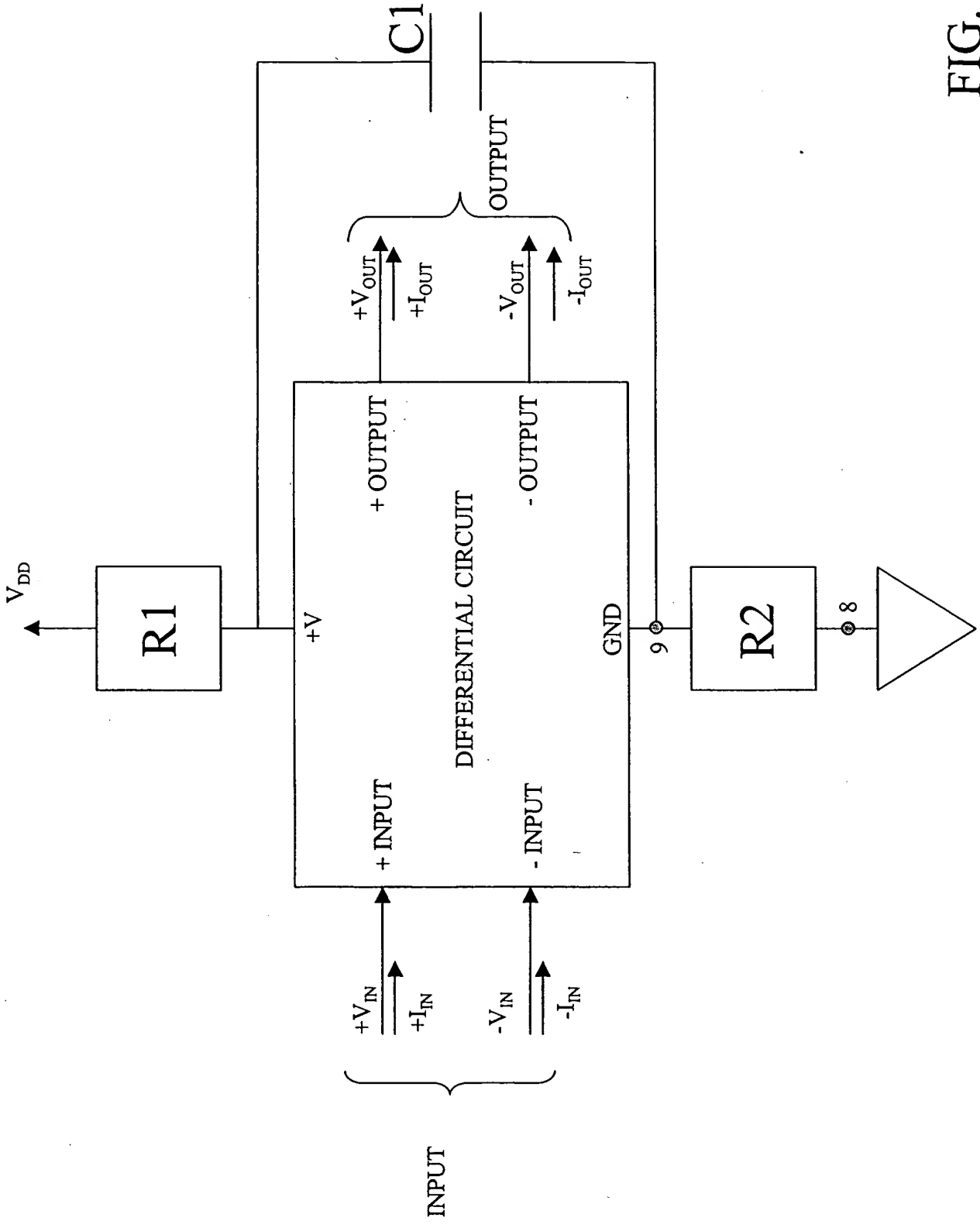


FIG. 406

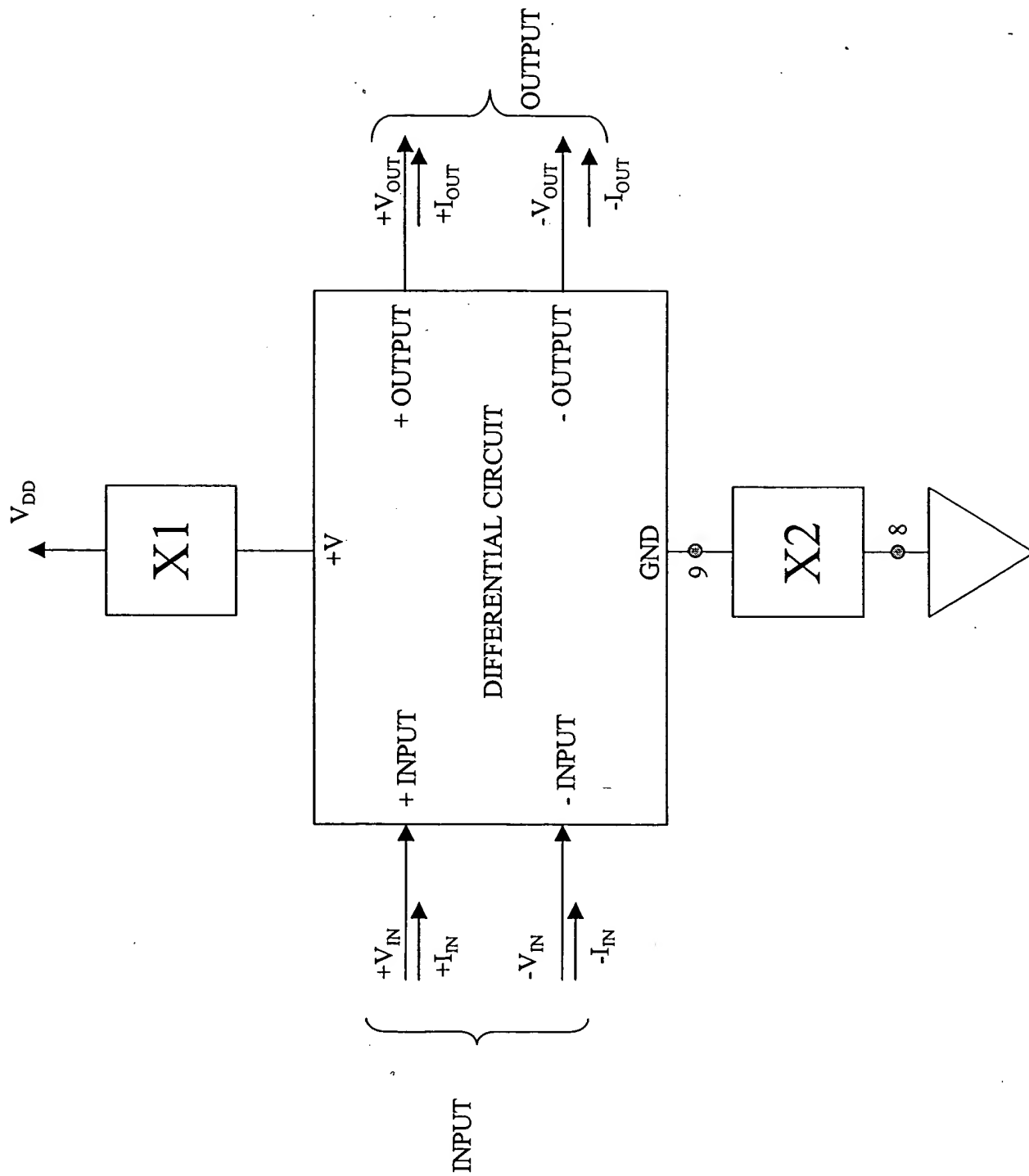


FIG. 48c

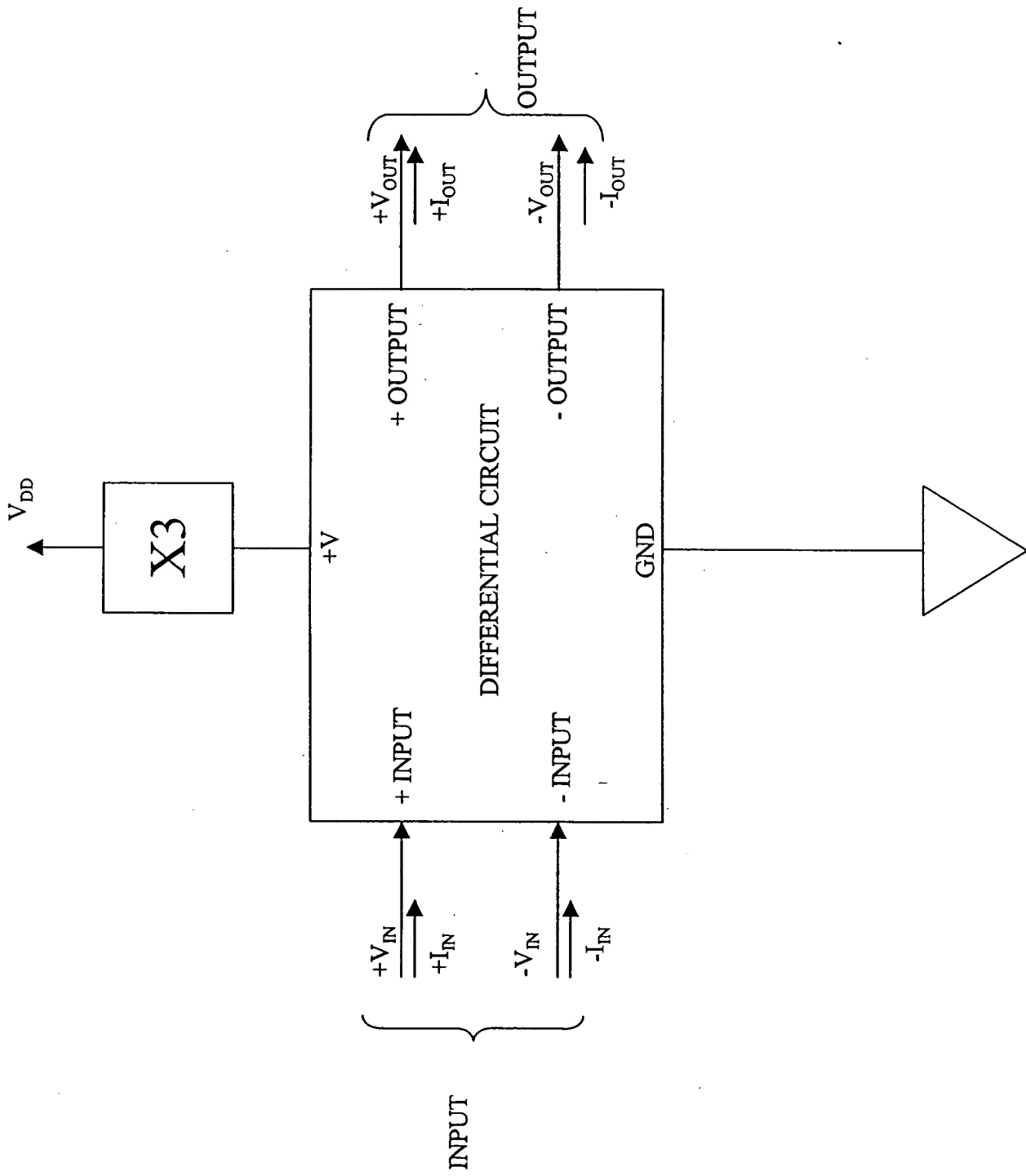


FIG. 48d

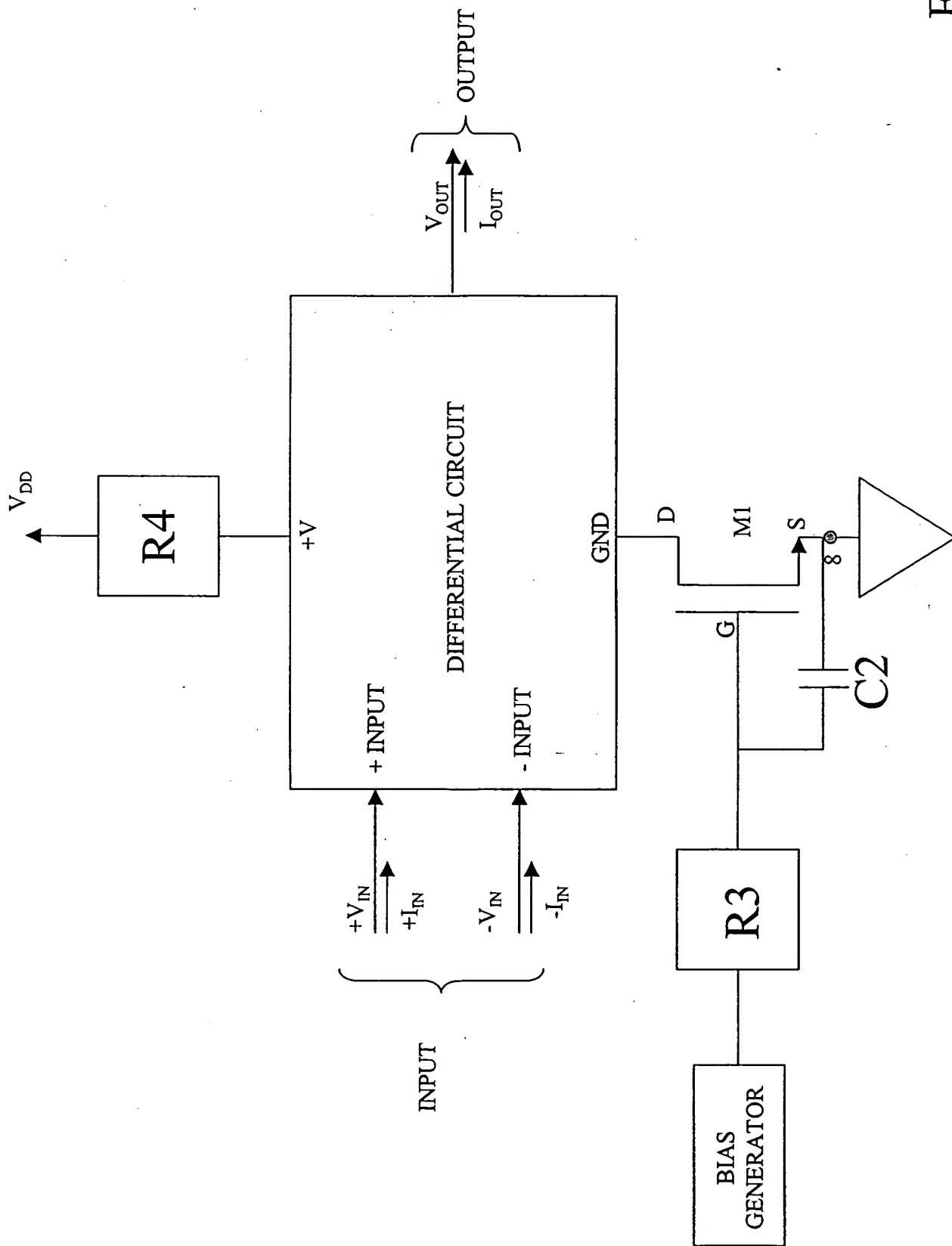


FIG. 48e

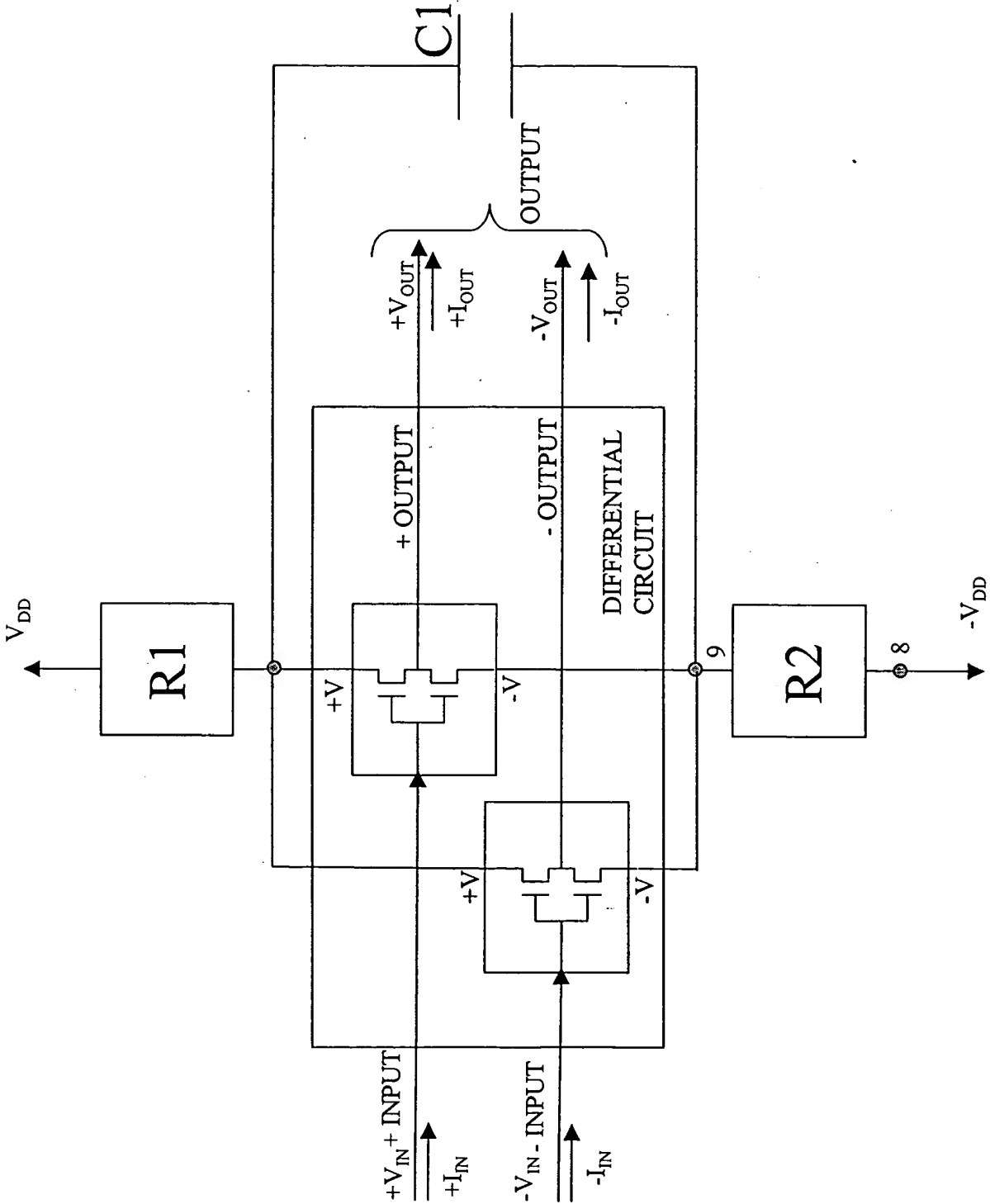


FIG. 48f